K510 Datasheet

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Preface

Purpose

This document describes the features, logical structures, functions, operating modes, and related registers of each module about K510. It also describes the interface timings and related parameters, the pins, pin usages, performance parameters, and package dimension of K510 in detail.

Intended Audiences

The document is intended for:

- Design and maintenance personnel for electronics.
- Sales personnel for electronic parts and components.

Revision History

Revision	Changes	Date
V1.0.0	Initial release	20210525

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1. Understand K510

1.1. K510 Introduction

Canaan K510 is an AI inference chip for edge systems, with the computing power of 3TFlOPS. It supports the AI applications for image and voice processing.

- Integrate the dual-core RISC-V CPU and Digital Signal Processor (DSP) with frequency up to 800 MHz. And Float Point Unit (FPU) is supported.
- Integrate the latest generation of ISP, which supports 2D noise reduction, 3D noise reduction, wide dynamic range, fish-eye correction, lens shading correction, and more features.
- Adopt Knowledge Processing Unit (KPU) for deep learning. Rich peripherals and memory interfaces are included for different applications.

1.2. Applications

Canaan K510 can be used in the following scenarios or products:

- Smart communities, such as face recognition, license plate recognition, and smart intercom.
- Vehicle after-market installation, such as driver micro-expression monitoring and analysis, road condition detection, and car-reversing rear view.
- Smart homes, such as sweeping robots and service robots.
- New retails, such as face detection, trajectory line analysis, behavior analysis, and facial recognition payment
- Intelligent video conference systems
- Smart pension
- Intelligent manufacturing

1.3. Features

The following figure shows the functional blocks of K510.

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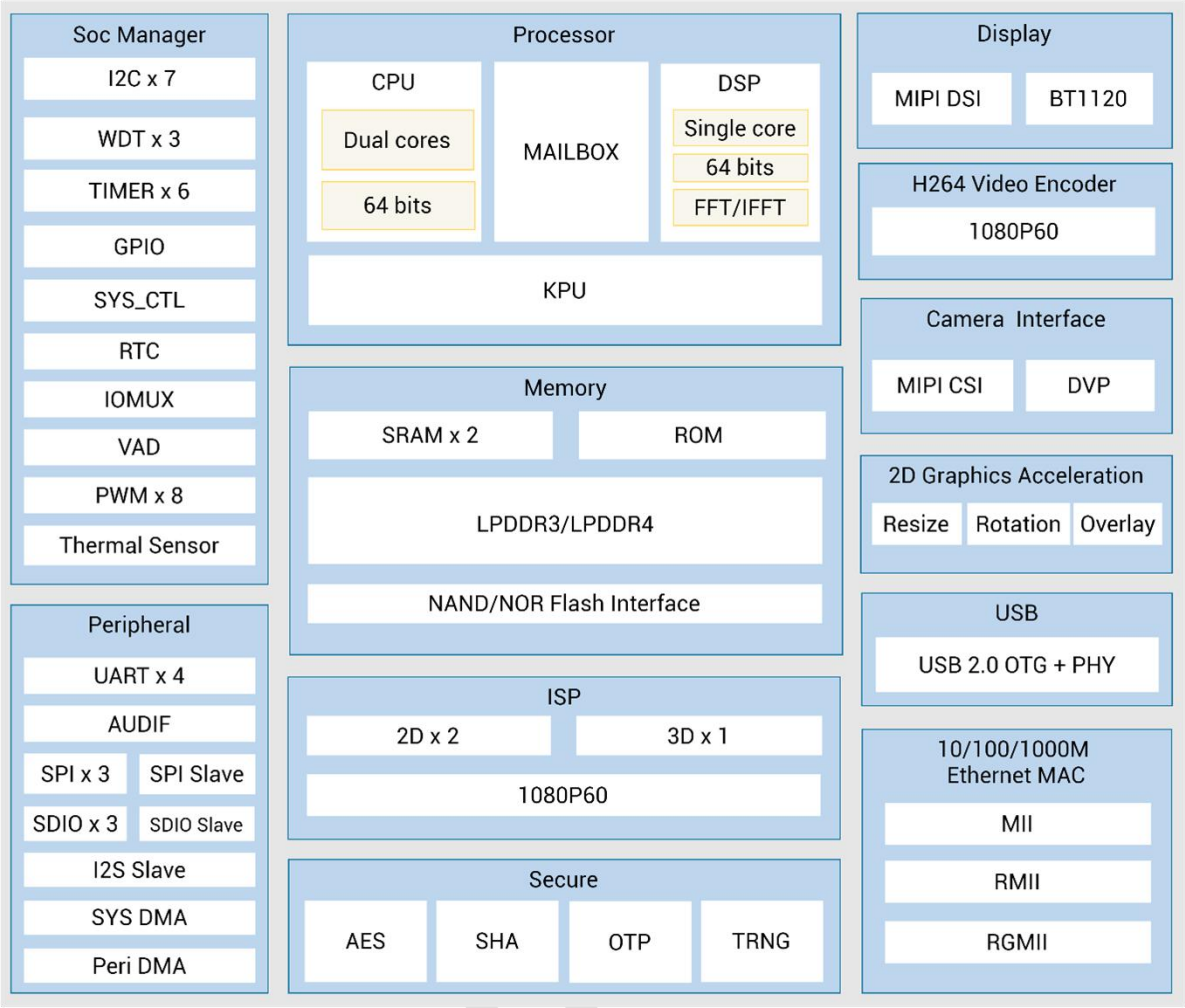

Figure 1-1 Block Diagram

1.3.1. Processor

CPU

CPU carries out applications and services.

- Working frequency: 800 MHz
- Core: 64-bit RISC-V
- Core number: 2
- ICACHE=32KB, DCACHE=32KB
- ICACHE four-way associativity
- DCACHE four-way associativity

- I/D cache Pseudo-LRU replacement policy
- Double-precision floating point extension
- L2 CACHE=256KB
- Machine mode, supervisor mode, user mode

DSP

DSP can carry standalone and run on RTOS.

- Working frequency: 800 MHz
- Core: 64-bit RISC-V and DSP extension
- Core number: 1
- ITCM = 128KB
- DTCM = 256KB
- ICACHE four-way associativity
- DCACHE four-way associativity
- I/D cache pseudo LRU replacement policy
- ICACHE=32KB, DCACHE=32KB
- Double-precision floating point extension
- Machine mode

1.3.2. AI Subsystem

KPU

KPU is responsible for computational acceleration. The majority of compute effort for deep learning inference is based on mathematical operations, such as convolutions, activation, pooling, normalization, and element wise. For a given network, the KPU compiler can well break down the whole computation into basic operators and ensure the efficiency of computation.

KPU supports the followings:

- NCHW mode input
- Weight of fixed-point Qint 8, Qint 6, Qint 4, and BF 16

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- Data precision BF16 and Qint8, and data foramt of FP 32, BF 16, and Qint 8
- Lossless compression and decompression
- Different data reuse strategies: weight reuse, input feature graph reuse, and output feature graph reuse
- Convolution, deconvolution, dilated convolution, matrix multiplication, and vector operation
- Different kinds of pooling operations, activation operations, and elementwise operations
- Any dimension of transpose, ROI align, and interpolation

FFT

Canaan K510 provides a Decimation-in-time (DIT) Radix-2 FFT/IFFT.

- FFT supports 64/128/256/512 points input data with 32/64 bits real and imaginary part.
- Only AX25P can write input data or read output data point by point.

Tip: DMA transactions are not supported.

1.3.3. Memory

The memory block consists of SRAM0, SARM1, and DDR.

SRAM0

The SRAM0 size is 1MB, and the base address is 0x8000_0000. The memory blocks inside SRAM0 are divided into the following two parts:

- 0x8000_0000 - 0x8001_FFFF: This is an 'always-on' block which is always available.
- 0x8002_0000 - 0x800F_FFFF: You can configure System Control to switch this block off to save power.

SRAM1

The SRAM1 size is 512KB.You can switch off SRAM1 by configuring System Control to save power.

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DDR

DDR mainly supports LPDDR3 and LPDDR4. The highest frequency about LPDDR3 is 2133 Mbps and LPDDR4 is 2700 Mbps. The connections between controller and PHY obey the DFI4.0 protocol.

DDR supports the followings:

- LPDDR3 - x16 bits and x32 bits
- LPDDR4 - x32-bit and dual-channel devices. The burst length could be 16 or 32.
- Configurable address mapping. It supports a wide range of memory size, including 1GB - 32 Gb for LPDDR3 and 4 Gb-32 GB for LPDDR4.
- A programmable register interface
  used to control memory parameters and protocols, including auto pre-charge.
- Full initialization of memory on controller reset.
- Advanced bank look-ahead features for high memory throughput
- Multiple low power modes, including data retention
- Dynamic frequency scaling
- Firmware-based training
- Integration of Deskew PLL and analog DLLs in the PHY
- BIST for external DRAM memories
- IO JTAG BSR Test, at speed internal loopback test capabilities

1.3.4. Peripheral Subsystem

UART

K510 contains 4 UARTs. Each one supports:

- RS485 interface (DE high available, RE low available)
- IrDA 1.0 SIR infrared mode
- 9-bit data mode
- 16750-compatible auto flow control mode

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- Programmable Transmitter Hold Register Empty (THRE)
- Baud clock reference output (baudout_n) pin
- Shadow registers (nine additional registers that shadow some of the existing register bits)
- Fully 16550 compatible
- Fractional Baud Rate Divisor (4-bit)
- Internal RX, TX FIFO depth is 32

I2S

The I2S slave controller supports:

- 4 channel TX and RX
- FIFO depth 16
- max 32-bit of word size
- FIFO threshold support

SPI

K510 contains 3 SPI master controllers and 1 SPI slave controller in the peripheral sub system. SPI supports:

- AHB interface with 32-bit data width
- DMA control
- Programmable delay
- Positive/Negative clock edge
- Programmable bit rate, clock stretching, and data size
- Configurable FIFO depth 32, slave select, and data pre-fetch

GPIO

The GPIO supports:

- 32-bit IO width
- IO debounce

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- IO triggered interrupts
- IO both edge interrupts

Temperature Sensor

Temperature sensor has high accuracy and low power consumption. It mainly supports the following features:

- ±3℃ untrimmed accuracy (-40℃ to 100℃)
- Digital interface
- 12-bit resolution
- Power management
- Silicon characterization
- Thermal management

USB

USB-HS core is a USB OTG dual-role device controller for a single peripheral device. The functions are as defined in the On-The-Go Supplement to the USB Power Delivery Specification v1.3 and v2.0.

SD

The SD sub-system includes 3 SD hosts and 1SD slave block.

- The host controllers serve the devices compatible with SD memory v4.0 (SD, SDHC, SDXC), SDIO v4.0, and MMC/eMMC v5.1.
- The slave controller meets the SDIO Card Specification v3.0. It is suitable for the I/O card applications like WLAN, and bluetooth with low power consumption. The controller supports SPI, 1-bit SD, 4-bit SD for embedded devices.

1.3.5. Video

The video subsystem is used for image and video processing. By real-time processing of the image sensor signal, a restored and enhanced digital image is obtained, making it closer to the image in reality.

The video subsystem mainly includes the following features:

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- VI supports 1 serial interface (MIPI) and 1 parallel interface (DVP)
  - MIPI interface:
    - ✓ MIPI DPHY 1.2 Receiver compliant
    - ✓ Configurable as two 1 Clock Lane and 2 Data Lanes channels (1x2) or one 1 Clock Lane and 4 Data Lanes channel (1x4)
  - DVP interface:
    - ✓ RAW 8/10/12/14-bit and YUV422
    - ✓ BT656 and BT1120 interfaces
- Two 2D ISPs:
  - Full version 2D ISP:
    - ✓ Lens shadow correction
    - ✓ Black level correction
    - ✓ White balance
    - ✓ Bad Pixel detection and correction
    - ✓ 2D Noise reduction
    - ✓ 3D noise reduction
    - ✓ 2-frame/3-frame HDR
    - ✓ Multi-CFA demosaic
    - ✓ Color correction matrix
    - ✓ RGB Gamma
    - ✓ Color space conversion
    - ✓ Local/global tone mapping
    - ✓ Sharpen
    - ✓ Post processing
    - ✓ Lens distortion correction

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- ✓ Hardware 3A Processing
- ✓ Scaler

- Reduced version 2D ISP:
  - ✓ No WDR and 3DNR compared with Full 2D ISP

- TOF ISP:
  - Support TOF sensor and generate depth images and gray images
  - Support CWM and PWM TOF sensor
  - Support IR sensor and process gray image
  - 2D noise reduction
  - Post processing
  - Hardware AE Processing and AE histogram
- FBC performs lossless compression of ISP output before being written to external memory to reduce bandwidth.
- Max resolution and frame rate is 1920x1080@60fps

1.3.6. Video Encoder (H264)

H264 is a video encoder engine designed to process video streams using the AVC (ISO/IEC 14496-10 Advanced Video Coding) standard.

It also supports JPEG encoding using ISO/IEC 10918-1(CCITT T.81) baseline process(DCT sequential) standard.

1.3.7. Audio

The audio interface supports the following features:

- PDM audio
  - PDM audio input/output, with data sampling rate of 2.048/2.8224 MHz, 1bit data width , sampling clock rate of 2.048/2.8224 MHz, and PCM sampling rate of 16kHz/44.1kHz
  - 1-8 IOs used to input and output PDM audio

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- The input and output can be configured with 1-8 PDM channels. It supports left/right mono mode and dual mode of PDM. All IO channel modes are unified. The max number of IO in dual mode is 4.
- The serial numbers of enabled channels are from small to big. Random enabling of each channel is not supported.
- PDM input data can be delayed up to 3 PCLK cycles.
- Conversion from input PDM audio data to PCM audio data
- Conversion from PCM audio data to PDM audio data for output

■ TDM Audio

- PCM audio in TDM format. Both delay and non-delay modes are supported.
- TDM audio input/output data sampling rate of 48kHz, and data width supports 16 bits (12/16 bits valid) and 32 bits (20/24/32 bits valid).
- 1/2/3/4/6/8/12 IOs used to input TDM audio data, and 1 IO used to output TDM audio data.
- 0-15 TDM channels can be configured for each input IO, and the biggest channel number for each channel is 24/IO number;Total input channel number cannot over 24.
- Sampling clock rate for each input IO: [(Number of channels+1)/2]×2×32×0.048MHz(A microphone can only count even channels.)
- 1-8 channels can be configured for output

■ I2S audio

- PCM audio in I2S Phillips format
- I2S audio input/output with data sampling rate of 16kHz / 48kHz, and data width of 32 bits. The valid data width needs to be customized. The sampling clock rate supports 2× data width × data sampling rate.
- 4 configurable IO to input,and 4 IO tooutput I2S audio data. The full-duplex mode is supported.
- Each RX/ TX channel FIFO depth is 8. FIFO threshold can be configured.

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- Support master mode, which means clockand fsync(TDM)/ws(I2S) are output from audio.
- The input and output audio modes can be configured separately, but the input or output can only support one mode.
- APB2.0 interface used to configure registers, and read/write PCM data. The default frequency of configurable APB working clock PCLK is 62.5 MHz, and the data interface is 32bits.
- PCM data can be transferred by DMA. Burst length is 8 4-byte data.
- The audio module can start working again after being disabled and re-enabled.
- The audio module can start working again after asserting reset and de-asserting reset.

1.3.8. Security System

Security system includes the following sub-modules:

- OTP (One Time Program)
- PUF (Physical Un-clone Function)
- AES (Advanced Encryption Standard)
- SHA (Secure Hash Algorithm)

1.3.9. EMAC

EMAC implements a 10/100/1000Mbps Ethernet MAC compatible with the IEEE 802.3 standard. EMAC can operate in either half or full duplex. The network configuration register is used to select the speed, duplex mode, and interface type (RMII or RGMII). EMAC supports the following features:

- MII/RMII/RGMII interface
- 10Mbps/100Mbps/1000Mbps speed
- Loopback mode
- Half duplex and full duplex operation
- Multiple address filtering modes

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- Support the insertion of checksums when transmitting frames.
- Support checking the checksum when receiving and discarding the error frame automatically.
- Support 802.3Qav, 802.3Qbv.
- 3 DMA queues. Transmit buffer is 8KB, 4KB and 4KB respectively, and receive buffer is 8KB.
- Support IEEE 1588-2002 (v1), 1588-2008 (v1 and v2) Standards for Precision Clock Synchronization Protocol.
- AHB master bus interface
- APB slave bus interface

1.3.10. Display

The display subsystem drives display devices such as LCD to display images and videos. It mainly includes the following features:

- Support up to 8 display layers which support alpha blending.
- Support configurable color space conversion, gamma correction, and dither.
- Support MIPI interface(up to 4 lanes), which is MIPI DPHY 1.2 compliant.
- Support 2D hardware accelerator which supports video layer scaler, OSD layer alpha-blending, and 90/270 degree rotation.
- Support BT1120 interface for multi-chip interconnection or debug by transforming to HDMI interface.
- Max resolution and frame rate is 1920x1080@60fps.

1.3.11. System

Mailbox

Mailbox works as an intermediate module to support the communicates between CPU, DSP and other sub-modules. It mainly involves the following functions.

- CPU and DSP shake hands with each other, share storage resources through hardware mutual exclusion (interlock) mechanism.

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- CPU and DSP modules configure registers for each sub-module.
- CPU and DSP query and read sub-module status information.

SDMA

SDMA supports transferring between DDR and SRAM.

- There are 4 channels for transferring different transactions, with 64 bytes data buffer per channel.
- Single-line, rectangular block, and linked list modes are provided for each DMA channel.
- Low power IDLE state of each channel can be set by shutting down corresponding clock.
- A 64-bit AXI4 master is used to transfer different channel transactions. The priority of each transaction is configured with each channel. Higher priority transaction gets higher chance to be transferred.
- Data address can be accessed in byte aligned.
- DMA controller works asynchronously with APB configuration part.

PDMA

PDMA supports transferring between peripheral port and DDR/SRAM.

- There are 16 channels for transferring different transactions, with 32 bytes data buffer per channel. 35 or less peripheral ports are supported by configuration for each channel.
- Low power IDLE state of each channel can be set by shutting down corresponding clock.
- A 64-bit AXI4 master is used to transfer different channel transactions.
- The priority of each transaction is configured with each channel. Higher priority transaction gets higher chance to be transferred.
- Peripheral data address can only be accessed in 4 bytes aligned with strobe signal to indicate lower 1/2/4 byte(s) are used, and only the fixed address is supported.
- DDR/SRAM data address width is 8 bytes, SRAM data address is 8 bytes aligned, and DDR data address is byte aligned. Only incremental burst address is supported.
- DMA controller works asynchronously with the APB configuration part.

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IOMUX

IOMUX maps the IOs of different functions inside the chip, and maps IO to the actual physical PAD. It supports the following features:

- Eight independent IOs (RESETN, CLK_25M, CLK_25M_OUT, CLK_32K, CLK_32K_OUT, TEST_EN1, TEST_EN0, and OTP_BYPASS) and 128 multiplexed IOs (IO_0~IO_127)
- Four types of PAD
- Access address: Base address is 0x9704_0000. The address space is 512 bytes (0x9704_0000~ 0x9704_01FF). Each physical PAD is allocated a 4-byte address space, that is, 32-bit configurable register.

  Tip: If the address is out of bounds, it will be rolled back.
- APB3.0 interface (The PREADY interface is always 1)
- 32-bit register per IO
- Working frequency: IOMUX is a combinational logic, Its configuration bus is APB with programmable PCLK clock frequency.
- Multi-plexed IO
  - In functional mode, MAIX2 supports three high-speed IO modes and one low-speed IO mode. In the low-speed IO mode, it can select 128 types of low speed pins from 191 types according to system configuration. The 128 pins will be taken as PAD IO interfaces.
  - The test mode supports four sub-modes: scan1_mode, scan2_mode, an_test_mode, and rambist_mode.

RTC

RTC mainly consists the calendar, stopwatch, and periodically wakeup functions.

- The calendar can display the year, month, day, week, hour, minute, second in real time.
- The stopwatch can touch off timing interrupt.
- The periodically wakeup can wake up the system at a specified time point.

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The RTC has the independent power to continue to work when the system is power-off. It has external crystal oscillator clock source (crystal oscillator frequency is 32768 Hz=2^15 Hz). Therefore, it can provide accurate time benchmark for the system.

SYS_CTL

SYS_CTL provides clock signals and reset signals for Maix2 SoC, assisting the software to complete the switching power-on and power-off status of each power domain. SYS_CTL supports:

- Management of SoC built-in PLL
- Management of the startup process and initialization of SOC after power on
- Sense of the working state of SOC core
- Control the dynamic switching of SOC between different power consumption modes

VAD

VAD detects the presence or absence of voices. The detection can be used to wake up the system from deep sleep by interruption. It supports 512kHz PDM and 16kHz PCM (in I2S Phillips format or delay/non-delay TDM format) voice data from microphones. Left or right channel voice data can be chosen by configuration.

WDT

There are 3 watch dog timers which can be used to prevent system lockup that may be caused by conflicting parts or programs in an SoC.

TIMER

There are 6 32-bit width timers connected to a APB bus.

PWM

There are two independent 4-bit Pulse Width Modulation generators, each can generate multiple types of waveform.

1.3.12. Boot

K510 can boot from:

- External SPI NAND flash

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- External eMMC
- External SDcard
- UART

During reset, the boot mode of the K510 depends on the values of the BOOT_CTL0 and BOOT_CTL1.

BOOT_CTL0	BOOT_CTL1	Boot Mode
0	0	UART
1	0	SDcard
0	1	SPI NAND flash
1	1	eMMC

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2. Package Information

2.1. Top Marking

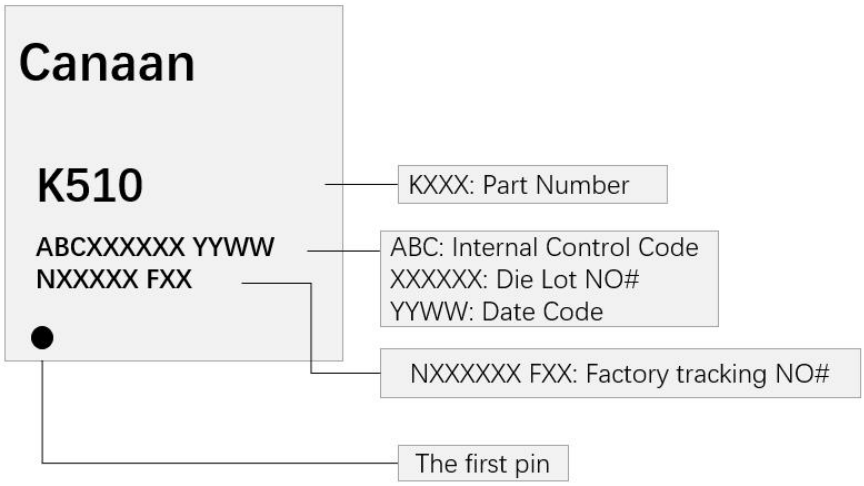


Figure 2-1 Package Definition

2.2. Dimension

The K510 uses VFBGA 14mm x14mm with 551 pins and 0.5mm pitch.

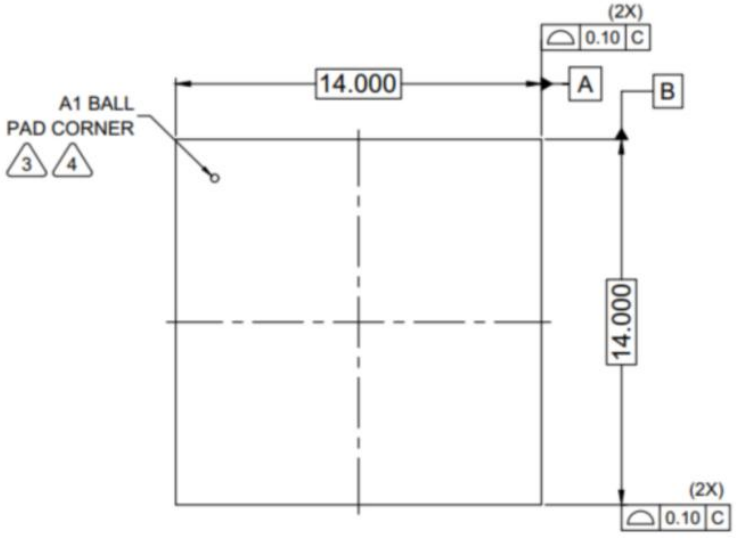


Figure 2-2 Top View

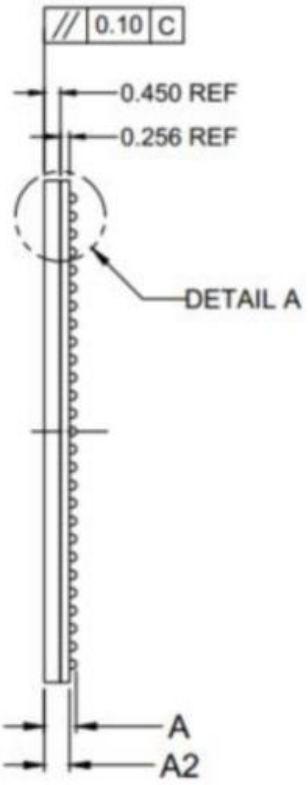


Figure 2-3 Side View

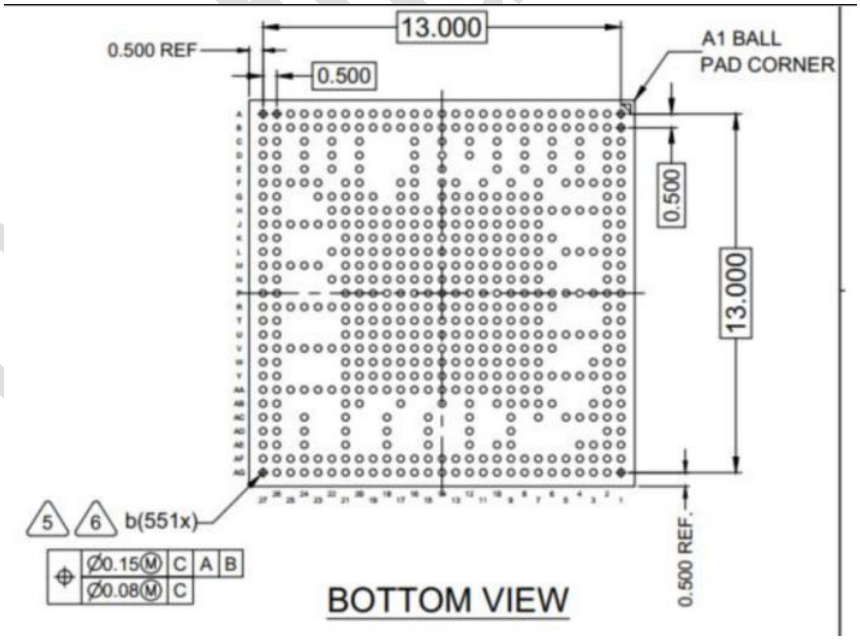
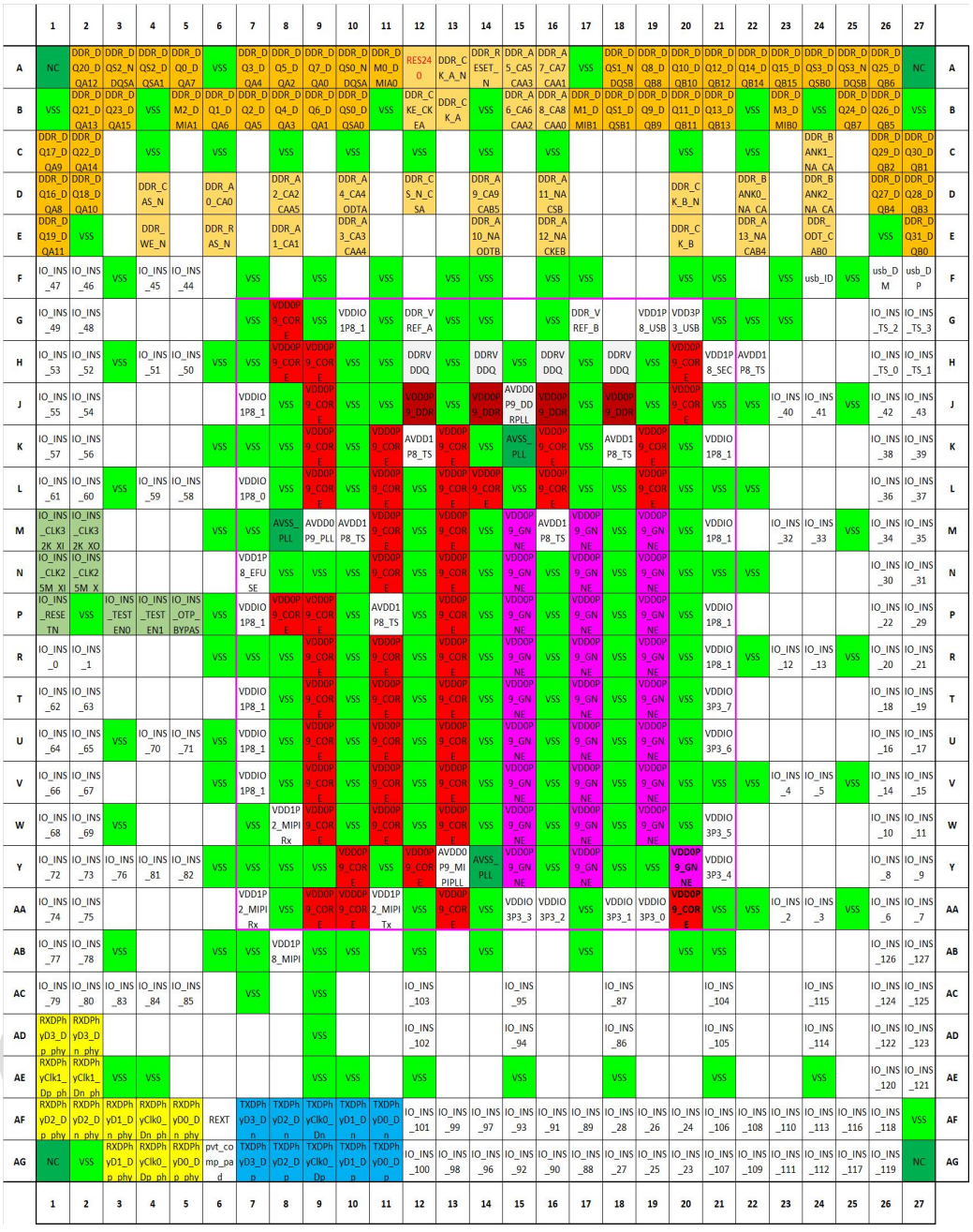


Figure 2-4 Bottom View

2.3. Ball Map



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	
A	NC	DDR_DQ20_DQA12	DDR_DQS2_NDQSA	DDR_DQS2_DQSA1	DDR_DQ0_DQA7	VSS	DDR_DQ3_DQA4	DDR_DQ5_DQA2	DDR_DQ7_DQA0	DDR_DQS0_NDQSA	DDR_DM0_DMIA0	RES240	DDR_CK_A_N	DDR_RESET_N	DDR_A5_CA5CAA3	DDR_A7_CA7CAA1	VSS	DDR_DQS1_NDQSB	DDR_DQ8_DQB8	DDR_DQ10_DQB10	DDR_DQ12_DQB12	DDR_DQ14_DQB14	DDR_DQ15_DQB15	DDR_DQS3_DQSB0	DDR_DQS3_NDQSB	DDR_DQ25_DQB6	NC	A
B	VSS	DDR_DQ21_DQA13	DDR_DQ23_DQA15	VSS	DDR_DM2_DMIA1	DDR_DQ1_DQA6	DDR_DQ2_DQA5	DDR_DQ4_DQA3	DDR_DQ6_DQA1	DDR_DQS0_DQSA0	VSS	DDR_CKE_CKEA	DDR_CK_A	VSS	DDR_A6_CA6CAA2	DDR_A8_CA8CAA0	DDR_DM1_DMIB1	DDR_DQS1_DQSB1	DDR_DQ9_DQB9	DDR_DQ11_DQB11	DDR_DQ13_DQB13	VSS	DDR_DM3_DMIB0	VSS	DDR_DQ24_DQB7	DDR_DQ26_DQB5	VSS	B
C	DDR_DQ17_DQA9	DDR_DQ22_DQA14		VSS		VSS		VSS		VSS		VSS		VSS		VSS				VSS		VSS		DDR_BANK1_NA_CA		DDR_DQ29_DQB2	DDR_DQ30_DQB1	C
D	DDR_DQ16_DQA8	DDR_DQ18_DQA10		DDR_CAS_N		DDR_A0_CA0		DDR_A2_CA2CAA5		DDR_A4_CA4ODTA		DDR_CS_N_CSA		DDR_A9_CA9CAB5		DDR_A11_NACSB				DDR_CK_B_N		DDR_BANK0_NA_CA		DDR_BANK2_NA_CA		DDR_DQ27_DQB4	DDR_DQ28_DQB3	D
E	DDR_DQ19_DQA11	VSS		DDR_WE_N		DDR_RAS_N		DDR_A1_CA1		DDR_A3_CA3CAA4				DDR_A10_NAODTB		DDR_A12_NACKEB				DDR_CK_B		DDR_A13_NACAB4		DDR_ODT_CAB0		VSS	DDR_DQ31_DQB0	E
F	IO_INS_47	IO_INS_46	VSS	IO_INS_45	IO_INS_44		VSS		VSS		VSS		VSS	VSS		VSS	VSS			VSS	VSS		VSS	usb_ID	VSS	usb_DM	usb_DP	F
G	IO_INS_49	IO_INS_48					VSS	VDDOP9_CORE	VSS	VDDIO1P8_1	VSS	DDR_VREF_A	VSS	VSS		VSS	DDR_VREF_B		VDD1P8_USB	VDD3P3_USB	VSS	VSS	VSS			IO_INS_TS_2	IO_INS_TS_3	G
H	IO_INS_53	IO_INS_52	VSS	IO_INS_51	IO_INS_50	VSS	VSS	VDDOP9_CORE	VDDOP9_CORE	VSS	VSS	DDRVDDQ	VSS	DDRVDDQ	VSS	DDRVDDQ	VSS	DDRVDDQ	VSS	VDDOP9_CORE	VDD1P8_SEC	AVDD1P8_TS				IO_INS_TS_0	IO_INS_TS_1	H
J	IO_INS_55	IO_INS_54					VDDIO1P8_1	VSS	VDDOP9_CORE	VSS	VSS	VDDOP9_DDR	VSS	VDDOP9_DDR	AVDD0P9_DDRPLL	VDDOP9_DDR	VSS	VDDOP9_DDR	VSS	VDDOP9_CORE	VSS	VSS	IO_INS_40	IO_INS_41	VSS	IO_INS_42	IO_INS_43	J
K	IO_INS_57	IO_INS_56				VSS	VSS	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	AVDD1P8_TS	VDDOP9_CORE	VSS	AVSS_PLL	VDDOP9_CORE	VSS	AVDD1P8_TS	VDDOP9_CORE	VSS	VDDIO1P8_1					IO_INS_38	IO_INS_39	K
L	IO_INS_61	IO_INS_60	VSS	IO_INS_59	IO_INS_58		VDDIO1P8_0	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VSS	VDDOP9_CORE	VSS	VSS	VSS				IO_INS_36	IO_INS_37	L
M	IO_INS_CLK32K_XI	IO_INS_CLK32K_XO				VSS	VSS	AVSS_PLL	AVDD0P9_PLL	AVDD1P8_TS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	AVDD1P8_TS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDIO1P8_1		IO_INS_32	IO_INS_33	VSS	IO_INS_34	IO_INS_35	M
N	IO_INS_CLK25M_XI	IO_INS_CLK25M_X					VDD1P8_EFUSE	VSS	VSS	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VSS	VSS				IO_INS_30	IO_INS_31	N
P	IO_INS_RESETN	VSS	IO_INS_TESTEN0	IO_INS_TESTEN1	IO_INS_OTP_BYPAS	VSS	VDDIO1P8_1	VDDOP9_CORE	VDDOP9_CORE	VSS	AVDD1P8_TS	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDIO1P8_1					IO_INS_22	IO_INS_29	P
R	IO_INS_0	IO_INS_1				VSS	VSS	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDIO1P8_1	VSS	IO_INS_12	IO_INS_13	VSS	IO_INS_20	IO_INS_21	R
T	IO_INS_62	IO_INS_63					VDDIO1P8_1	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDIO3P3_7					IO_INS_18	IO_INS_19	T
U	IO_INS_64	IO_INS_65	VSS	IO_INS_70	IO_INS_71	VSS	VDDIO1P8_1	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDIO3P3_6					IO_INS_16	IO_INS_17	U
V	IO_INS_66	IO_INS_67				VSS	VDDIO1P8_1	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VSS	VSS	IO_INS_4	IO_INS_5	VSS	IO_INS_14	IO_INS_15	V
W	IO_INS_68	IO_INS_69	VSS				VSS	VDD1P2_MIPIRx	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VDDIO3P3_5					IO_INS_10	IO_INS_11	W
Y	IO_INS_72	IO_INS_73	IO_INS_76	IO_INS_81	IO_INS_82	VSS	VSS	VSS	VSS	VDDOP9_CORE	VSS	VDDOP9_CORE	AVDD0P9_MIPIPLL	AVSS_PLL	VDDOP9_GNNE	VSS	VDDOP9_GNNE	VSS	VSS	VDDOP9_GNNE	VDDIO3P3_4					IO_INS_8	IO_INS_9	Y
AA	IO_INS_74	IO_INS_75					VDD1P2_MIPIRx	VSS	VDDOP9_CORE	VDDOP9_CORE	VDD1P2_MIPITx	VSS	VDDOP9_CORE	VSS	VDDIO3P3_3	VDDIO3P3_2	VSS	VDDIO3P3_1	VDDIO3P3_0	VDDOP9_CORE	VSS	VSS	IO_INS_2	IO_INS_3	VSS	IO_INS_6	IO_INS_7	AA
AB	IO_INS_77	IO_INS_78	VSS			VSS	VSS	VDD1P8_MIPI	VSS	VSS		VSS		VSS			VSS			VSS	VSS					IO_INS_126	IO_INS_127	AB
AC	IO_INS_79	IO_INS_80	IO_INS_83	IO_INS_84	IO_INS_85		VSS		VSS			IO_INS_103			IO_INS_95			IO_INS_87			IO_INS_104			IO_INS_115		IO_INS_124	IO_INS_125	AC
AD	RXDPhyD3_Dp_phy	RXDPhyD3_Dn_phy							VSS			IO_INS_102			IO_INS_94			IO_INS_86			IO_INS_105			IO_INS_114		IO_INS_122	IO_INS_123	AD
AE	RXDPhyClk1_Dp_ph	RXDPhyClk1_Dn_ph	VSS	VSS					VSS	VSS		VSS			VSS			VSS			VSS			VSS		IO_INS_120	IO_INS_121	AE
AF	RXDPhyD2_Dp_phy	RXDPhyD2_Dn_phy	RXDPhyD1_Dn_phy	RXDPhyClk0_Dn_ph	RXDPhyD0_Dn_phy	REXT	TXDPhyD3_Dn	TXDPhyD2_Dn	TXDPhyClk0_Dn	TXDPhyD1_Dn	TXDPhyD0_Dn	IO_INS_101	IO_INS_99	IO_INS_97	IO_INS_93	IO_INS_91	IO_INS_89	IO_INS_28	IO_INS_26	IO_INS_24	IO_INS_106	IO_INS_108	IO_INS_110	IO_INS_113	IO_INS_116	IO_INS_118	VSS	AF
AG	NC	VSS	RXDPhyD1_Dp_phy	RXDPhyClk0_Dp_ph	RXDPhyD0_Dp_phy	pvt_comp_pad	TXDPhyD3_Dp	TXDPhyD2_Dp	TXDPhyClk0_Dp	TXDPhyD1_Dp	TXDPhyD0_Dp	IO_INS_100	IO_INS_98	IO_INS_96	IO_INS_92	IO_INS_90	IO_INS_88	IO_INS_27	IO_INS_25	IO_INS_23	IO_INS_107	IO_INS_109	IO_INS_111	IO_INS_112	IO_INS_117	IO_INS_119	NC	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	

Figure 2-4 Ball Map

2.4. Pin List

Pin#	Pin Name	Pin Type	Pin#	Pin Name	Pin Type	Pin#	Pin Name	Pin type
AA1	IO_INS_74	I/O	AF25	IO_INS_116	I/O	M24	IO_INS_33	I/O
AA2	IO_INS_75	I/O	AF26	IO_INS_118	I/O	M26	IO_INS_34	I/O
AA23	IO_INS_2	I/O	AG12	IO_INS_100	I/O	M27	IO_INS_35	I/O
AA24	IO_INS_3	I/O	AG13	IO_INS_98	I/O	N26	IO_INS_30	I/O
AA26	IO_INS_6	I/O	AG14	IO_INS_96	I/O	N27	IO_INS_31	I/O
AA27	IO_INS_7	I/O	AG15	IO_INS_92	I/O	P26	IO_INS_22	I/O
AB1	IO_INS_77	I/O	AG16	IO_INS_90	I/O	P27	IO_INS_29	I/O
AB2	IO_INS_78	I/O	AG17	IO_INS_88	I/O	R1	IO_INS_0	I/O
AB26	IO_INS_126	I/O	AG18	IO_INS_27	I/O	R2	IO_INS_1	I/O
AB27	IO_INS_127	I/O	AG19	IO_INS_25	I/O	R23	IO_INS_12	I/O
AC1	IO_INS_79	I/O	AG20	IO_INS_23	I/O	R24	IO_INS_13	I/O
AC12	IO_INS_103	I/O	AG21	IO_INS_107	I/O	R26	IO_INS_20	I/O
AC15	IO_INS_95	I/O	AG22	IO_INS_109	I/O	R27	IO_INS_21	I/O
AC18	IO_INS_87	I/O	AG23	IO_INS_111	I/O	T1	IO_INS_62	I/O
AC2	IO_INS_80	I/O	AG24	IO_INS_112	I/O	T2	IO_INS_63	I/O
AC21	IO_INS_104	I/O	AG25	IO_INS_117	I/O	T26	IO_INS_18	I/O
AC24	IO_INS_115	I/O	AG26	IO_INS_119	I/O	T27	IO_INS_19	I/O
AC26	IO_INS_124	I/O	F1	IO_INS_47	I/O	U1	IO_INS_64	I/O

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Pin#	Pin Name	Pin Type	Pin#	Pin Name	Pin Type	Pin#	Pin Name	Pin type
AC27	IO_INS_125	I/O	F2	IO_INS_46	I/O	U2	IO_INS_65	I/O
AC3	IO_INS_83	I/O	F4	IO_INS_45	I/O	U26	IO_INS_16	I/O
AC4	IO_INS_84	I/O	F5	IO_INS_44	I/O	U27	IO_INS_17	I/O
AC5	IO_INS_85	I/O	G1	IO_INS_49	I/O	U4	IO_INS_70	I/O
AD12	IO_INS_102	I/O	G2	IO_INS_48	I/O	U5	IO_INS_71	I/O
AD15	IO_INS_94	I/O	H1	IO_INS_53	I/O	V1	IO_INS_66	I/O
AD18	IO_INS_86	I/O	H2	IO_INS_52	I/O	V2	IO_INS_67	I/O
AD21	IO_INS_105	I/O	H4	IO_INS_51	I/O	V23	IO_INS_4	I/O
AD24	IO_INS_114	I/O	H5	IO_INS_50	I/O	V24	IO_INS_5	I/O
AD26	IO_INS_122	I/O	J1	IO_INS_55	I/O	V26	IO_INS_14	I/O
AD27	IO_INS_123	I/O	J2	IO_INS_54	I/O	V27	IO_INS_15	I/O
AE26	IO_INS_120	I/O	J23	IO_INS_40	I/O	W1	IO_INS_68	I/O
AE27	IO_INS_121	I/O	J24	IO_INS_41	I/O	W2	IO_INS_69	I/O
AF12	IO_INS_101	I/O	J26	IO_INS_42	I/O	W26	IO_INS_10	I/O
AF13	IO_INS_99	I/O	J27	IO_INS_43	I/O	W27	IO_INS_11	I/O
AF14	IO_INS_97	I/O	K1	IO_INS_57	I/O	Y1	IO_INS_72	I/O
AF15	IO_INS_93	I/O	K2	IO_INS_56	I/O	Y2	IO_INS_73	I/O
AF16	IO_INS_91	I/O	K26	IO_INS_38	I/O	Y26	IO_INS_8	I/O
AF17	IO_INS_89	I/O	K27	IO_INS_39	I/O	Y27	IO_INS_9	I/O

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Pin#	Pin Name	Pin Type	Pin#	Pin Name	Pin Type	Pin#	Pin Name	Pin type
AF18	IO_INS_28	I/O	L1	IO_INS_61	I/O	Y3	IO_INS_76	I/O
AF19	IO_INS_26	I/O	L2	IO_INS_60	I/O	Y4	IO_INS_81	I/O
AF20	IO_INS_24	I/O	L26	IO_INS_36	I/O	Y5	IO_INS_82	I/O
AF21	IO_INS_106	I/O	L27	IO_INS_37	I/O			
AF22	IO_INS_108	I/O	L4	IO_INS_59	I/O			
AF23	IO_INS_110	I/O	L5	IO_INS_58	I/O			
AF24	IO_INS_113	I/O	M23	IO_INS_32	I/O			

Table 2-1 Pin List

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3. Electrical Specification

3.1. Absolute Max Ratings

Parameter	Value	Unit
Storage Temperature	-65~125	℃
Operating Temperature	-40~85	℃
VDD0P9_CORE	-0.2~1.08	V
VDD0P9_GNNE	-0.2~1.08	V
VDD0P9_DDR	-0.2~1.08	V
DDRVDDQ	-0.2~1.32/1.44/1.62	V
AVDD0P9_DDRPLL	-0.2~1.08	V
VDD1P8_USB	-0.2~2.16	V
VDD3P3_USB	-0.2~3.96	V
AVDD0P9_PLL	-0.2~1.08	V
AVDD0P9_MIPIPLL	-0.2~1.08	V
VDD1P2_MIPITx	-0.2~1.32	V
VDD1P2_MIPIRx	-0.2~1.32	V
VDD1P8_MIPI	-0.2~2.16	V
VDD1P8_SEC	-0.2~2.16	V
VDD1P8_EFUSE	-0.2~2.16	V
AVDD1P8_TS	-0.2~2.16	V
VDDIO1P8_0	-0.2~2.16	V
VDDIO1P8_1	-0.2~2.16	V
VDDIO3P3_0	-0.2~2.16/3.96	V
VDDIO3P3_1	-0.2~2.16/3.96	V
VDDIO3P3_2	-0.2~2.16/3.96	V

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Parameter	Value	Unit
VDDIO3P3_3	-0.2~2.16/3.96	V
VDDIO3P3_4	-0.2~2.16/3.96	V
VDDIO3P3_5	-0.2~3.96	V
VDDIO3P3_6	-0.2~2.16/3.96	V
VDDIO3P3_7	-0.2~2.16/3.96	V

Table 3-1 Absolute Maximum Ratings

3.2. Recommended Operating Condition

Ball name	Min	Typ	Max	Units
VDD0P9_CORE	0.81	0.9	0.99	V
VDD0P9_GNNE	0.81	0.9	0.99	V
VDD0P9_DDR	0.81	0.9	0.99	V
DDRVDDQ	0.99/1.08/1.215	1.1/1.2/1.35	1.21/1.32/1.485	V
AVDD0P9_DDRPLL	0.81	0.9	0.99	V
VDD1P8_USB	1.62	1.8	1.98	V
VDD3P3_USB	2.97	3.3	3.63	V
AVDD0P9_PLL	0.81	0.9	0.99	V
AVDD0P9_MIPIPLL	0.81	0.9	0.99	V
VDD1P2_MIPITx	1.08	1.2	1.32	V
VDD1P2_MIPIRx	1.08	1.2	1.32	V
VDD1P8_MIPI	1.62	1.8	1.98	V
VDD1P8_SEC	1.62	1.8	1.98	V
VDD1P8_EFUSE	1.62	1.8	1.98	V
AVDD1P8_TS	1.62	1.8	1.98	V
VDDIO1P8_0	1.62	1.8	1.98	V

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Ball name	Min	Typ	Max	Units
VDDIO1P8_1	1.62	1.8	1.98	V
VDDIO3P3_0	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO3P3_1	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO3P3_2	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO3P3_3	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO3P3_4	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO3P3_5	2.97	3.3	3.63	V
VDDIO3P3_6	1.62/2.97	1.8/3.3	1.98/3.63	V
VDDIO3P3_7	1.62/2.97	1.8/3.3	1.98/3.63	V

Table 3-2 Recommended Operating Condition

3.3. DC Characteristics

3.3.1. Electrical Characteristics for General IO

For VDDIO1P8_0/VDDIO1P8_1, the DC Characteristics are as follows:

Parameter	Description	Min.	Type.	Max.	Units
V_{IL}	Input Low Voltage	-0.3		0.35*VDDIO	V
V_{IH}	Input High Voltage	0.65*VDDIO		1.98	V
V_{OL}	Output Low Voltage			0.45	V
V_{OH}	Output High Voltage	1.53			V
R_{PU}	Pull-up Resistor	60k	89k	137k	Ω
R_{PD}	Pull-down Resistors	1k	104k	196k	Ω

Table 3-3 Electrical characteristics for general IO (1)

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For VDDIO3P3_*, the DC Characteristics are as follows:

Parameter	Description	Min.	Type.	Max.	Units
V_{IL}	Input Low Voltage	-0.3		0.25*VDDIO	V
V_{IH}	Input High Voltage	0.625*VDDIO		3.465	V
V_{OL}	Output Low Voltage			0.125*VDDIO	V
V_{OH}	Output High Voltage	0.75*VDDIO			V
R_{PU}	Pull-up Resistor	33k	59k	91k	Ω
R_{PD}	Pull-down Resistors	34k	61k	108k	Ω

Table 3-4 Electrical Characteristics for General IO (2)

3.3.2. Electrical Characteristics for MIPI/CSI/DSI

- **DSI TX-DPHY HS Transmitter:**

Parameter	Description	Min	Norm	Max	Units	Notes
VCMTX	HS transmit static common modevoltage	150	200	250	mV	1
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV	2
|VOD|	HS transmit differential voltage	140	200	270	mV	1
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0			14	mV	2

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Parameter	Description	Min	Norm	Max	Units	Notes
VOHHS	HS output high voltage			360	mV	1
ZOS	Single ended output impedance	40	50	62.5	Ω	
ΔZOS	Single ended output impedance mismatch			10	%	

Table 3-5 Electrical characteristics for DSI TX-DPHY HS Transmitter

Notes:

- Value when driving into load impedance anywhere in the ZID range.
- A transmitter should minimize ΔVOD and ΔVCMTX(1,0) in order to minimize radiation, and optimize signal integrity.

■ **DSI TX-DPHY LP Transmitter:**

Parameter	Description	Min	Norm	Max	Units	Notes
VOH	Thevenin output high level	1.1	1.2	1.3	V	
VOL	Thevenin output low level	-50		50	mV	
ZOLP	Output impedance of LP transmitter	110			Ω	3,4

Table 3-6 Electrical characteristics for DSI TX-DPHY LP Transmitter

Notes:

- Applicable when the supported data rate <= 1.5 Gbps.

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- Applicable when the supported data rate > 1.5 Gbps.
- See Figure 46 and Figure 47 in MIPI DPHY 1.2 Specification .
- Though no maximum value for ZOLP is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

■ **DSI TX-DPHY LP Receiver:**

Parameter	Description	Min	Norm	Max	Units	Notes
VIH	Logic 1 input voltage	880			mV	1
		740			mV	2
VIL	Logic 0 input voltage, not in ULP State			550	mV	
VIL-ULPS	Logic 0 input voltage, ULP State			300	mV	
VHYST	Input hysteresis	25			mV	

Table 3-7 Electrical characteristics for DSI TX-DPHY LP Receiver

Notes:

- Applicable when the supported data rate <= 1.5 Gbps.
- Applicable when the supported data rate > 1.5 Gbps.

■ **CSI Tx-DPHY HS Receiver:**

Parameter	Description	Min	Norm	Max	Units	Note
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV	1,2

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VIDTH	Differential input high threshold			70	mV	3
				40	mV	4
VIDTL	Differential input low threshold	-70			mV	3
		-40			mV	4
VIHHS	Single-ended input high voltage			460	mV	1
VILHS	Single-ended input low voltage	-40			mV	1
VTERM-EN	Single-ended threshold for HS termination enable			450	mV	
ZID	Differential input impedance	80	100	125	Ω	

Table 3-8 Electrical characteristics for CSI Tx-DPHY HS Receiver

Notes:

- Excluding possible additional RF interference of 100mV peak sine wave beyond 450 MHz.
- This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450 MHz.
- For devices supporting data rates <= 1.5 Gbps.
- For devices supporting data rates > 1.5 Gbps

■ **CSI Tx-DPHY LP Receiver:**

Parameter	Description	Min	Norm	Max	Units	Notes
VIH	Logic 1 input voltage	880			mV	1
		740			mV	2

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Parameter	Description	Min	Norm	Max	Units	Notes
VIL	Logic 0 input voltage, not in ULP State			550	mV	
VIL-ULPS	Logic 0 input voltage, ULP State			300	mV	
VHYST	Input hysteresis	25			mV	

Table 3-9 Electrical Characteristics for CSI Tx-DPHY LP Receiver

Notes:

- Applicable when the supported data rate <= 1.5 Gbps.
- Applicable when the supported data rate > 1.5 Gbps.

3.3.3. Electrical Characteristics for DDR IO

■ **DC characteristics for LPDDR3:**

Symbol	Parameter	Condition	Min	Typ.	Max	Units
VDVDD	Power supply voltage	-	1.14	1.2	1.3	V
VREF	Input reference voltage	-	0.49* VDVDD	VDVDD/2	0.51* VDVDD	V
VREFODT	Input reference voltage – ODT Enabled	-	VODTR/2 - 0.01* VDVDD	VODTR/2	VODTR/2 +0.01* VDVDD	V
VREF-noise	Reference voltage noise	-	-1% of VDVDD	-	+1% of VDVDD	V
VTT	Termination voltage	-	-	VDVDD/2	-	V
RON34 [1]	Driver output impedance	VPAD=0.5*VDVDD	Typ-10%	34.3	Typ+10%	Ω

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Symbol	Parameter	Condition	Min	Typ.	Max	Units
RON40 [1]	Driver output impedance	VPAD=0.5*VDVDD	Typ-10%	40	Typ+10%	Ω
RON48 [1]	Driver output impedance	VPAD=0.5*VDVDD	Typ-10%	48	Typ+10%	Ω
RODT240 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	240	Typ+10%	Ω
RODT120 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	120	Typ+10%	Ω
RODT80 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	80	Typ+10%	Ω
RODT60 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	60	Typ+10%	Ω
RODT40 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	48	Typ+10%	Ω
RODT30 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	40	Typ+10%	Ω
RODT20 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	34	Typ+10%	Ω
ΔVM [1]	Deviation for RTT	VPAD=0.5*VDVDD	-5	-	5	%
VIH(DC)	DC input logic high	-	VREF+0.100	-	VDVDD	V
VIL(DC)	DC input logic low	-	VDVSS	-	VREF-0.100	V
VIH(AC)	AC input logic high	-	VREF+0.150	-	-	V
VIL(AC)	AC input logic low	-	-	-	VREF-0.150	V

Table 3-10 DC Characteristics for LPDDR3

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■ **DC characteristics for LPDDR4:**

Symbol	Parameter	Condition	Min	Typ.	Max	Units
VDVDD	Power supply voltage	-	1.06	1.1	1.17	V
VREF	Input reference voltage	Range 0	0.10* VDVDD	1.255* VDVDD	0.30* VDVDD	V
Range 1	0.22* VDVDD	0.272* VDVDD	0.42* VDVDD	V		
VREF-noise	Reference voltage noise	-	-1% of VDVDD	-	+1% of VDVDD	V
VTT	Termination voltage	-	-	VDVSS	-	V
RON [1]	Driver output impedance	VPAD=0.5*VDVDD	Typ-10%	34.3	Typ+10%	Ω
RODT240 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	240	Typ+10%	Ω
RODT120 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	120	Typ+10%	Ω
RODT80 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	80	Typ+10%	Ω
RODT60 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	60	Typ+10%	Ω
RODT40 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	48	Typ+10%	Ω
RODT30 [1]	ODT impedance	VPAD=0.5*VDVDD	Typ-10%	40	Typ+10%	Ω
VIH(DC)	DC input logic high	-	VREF+0.090	-	VDVDD	V
VIL(DC)	DC input logic low	-	VDVSS	-	VREF-0.090	V
VIH(AC)	AC input logic high	-	VREF+0.150	-	-	V

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Symbol	Parameter	Condition	Min	Typ.	Max	Units
VIL(AC)	AC input logic low	-	-	-	VREF-0.150	V

Table 3-11 DC Characteristics for LPDDR4

3.3.4. Electrical Characteristics for USB

■ **Operating conditions:**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VCC33A	Analog power supply	-	2.97	3.3	3.63	V
VCC18A	Analog power supply	-	1.62	1.8	1.98	V
VCC09D	Digital power supply	-	0.85	0.9	0.95	V
Vnoise_33A	Allowable power noise on analog supply	1Hz~100kHz	-	-	150	mV
Vnoise_18A	Allowable power noise on analog supply	1Hz~100kHz	-	-	150	mV
Vnoise_09D	Allowable power noise on digital supply	1Hz~100kHz	-	-	50	mV
IVCC33A	Operating current of VCC33A domain under different modes	HS mode (480Mbps)	-	0.8	1	mA
FSTX mode (12Mbps) (with 50pF load)	-	8.5	9.4	mA		
FSTX mode (12Mbps) (with 3m	-	23	25	mA		

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
cable)						
FSRX mode (12Mbps)	-	11	40	uA		
LSTX Mode (1.5Mbps) (with 600pF load)	-	4.2	5	mA		
LSRX Mode (1.5Mbps)	-	11	40	uA		
Suspend mode (Without pull-up resistor on the DP)	-	11	40	uA		
Suspend mode (With pull-up resistor on the DP)	-	220	300	uA		
IVCC18A	Operating current of VCC18A domain under different modes	HS mode (480Mbps)	-	30	36	mA
FSTX mode (12Mbps) (with 50pF load)	-	6.8	8.2	mA		
FSTX mode (12Mbps) (with 3m cable)	-	6.8	8.2	mA		
FSRX mode (12Mbps)	-	4	5	mA		

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
LSTX Mode (1.5Mbps) (with 600pF load)	-	5.5	6.6	mA		
LSRX Mode (1.5Mbps)	-	4	5	mA		
Suspend mode	-	0.2	75	uA		
IVCC09D	Operating current of VCC09D domain under different modes	HS mode (480Mbps)	-	6	9	mA
FSTX mode (12Mbps) (with 50pF load)	-	1.6	6.5	mA		
FSTX mode (12Mbps) (with 3m cable)	-	1.6	6.5	mA		
FSRX mode (12Mbps)	-	1.6	6.5	mA		
LSTX Mode (1.5Mbps) (with 600pF load)	-	1.6	6.5	mA		
LSRX Mode (1.5Mbps)	-	1.6	6.5	mA		
Suspend mode	-	100	2000	uA		
Ta	Operating Ambient Temperature	-	-40	-	85	℃

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Tj	Operating Junction Temperature	-	-40	-	125	℃

Table 3-12 Electrical Characteristics for USB Operating Conditions

■ **For digital pins:**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Input levels						
VIL	Low-level input voltage	-	-	-	0.8	V
VIH	High-level input voltage	-	2.0	-	-	V
Output levels						
VOL	Low-level output voltage	-	-	-	0.2	V
VOH	High-level output voltage	-	VCC - 0.2	-	-	V

Table 3-13 Electrical Characteristics for USB Digital Pins

■ **For DP/DM:**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
USB 2.0 transceiver (HS)						
Input levels						
VHSCM	High-speed data signaling common mode voltage range	-	-50	-	500	mV

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
VHSSQ	High-speed squelch detection threshold	Squelch detected	-	-	100	mV
No squelch detected	200	-	-	mV		
VHSDSC	High-speed disconnect detection threshold.	-	525	-	625	mV
Output levels						
VHSOI	High-speed idle level output voltage	-	-10	-	10	mV
VHSOL	High-speed low level output voltage	-	-10	-	10	mV
VHSOH	High-speed high level output voltage	-	360	400	440	mV
VCHIRPJ	Chirp-J output voltage (Differential)	-	700	-	1100	mV
VCHIRPK	Chirp-K output voltage (Differential)	-	-900	-	-500	mV
USB 1.1 transceiver (FS)						
Input levels						
VDI	Differential input sensitivity	|VI(DP) - VI(DM)|	0.2	-	-	V

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VCM	Differential common mode voltage	-	0.8	-	2.5	V
Input levels (Single-ended receiver)						
VIH	High (driven)	-	2.0	-	-	V
VIHZ	High (floating)	-	2.7	-	3.6	V
VIL	Low	-	-	-	0.8	V
Output levels						
VOL	Low-level output voltage	-	0	-	0.3	V
VOH	High-level output voltage	-	2.8	-	3.6	V
VCRS	Cross point of DP/DM	-	1.3	-	2.0	V
Terminations						
RPU_UP	Pull-up resistor on upstream ports	-	1.425	1.5	1.575	KΩ
RPU_DN	Pull-down resistor on downstream ports	-	14.25	15	15.75	KΩ

Table 3-14 Electrical Characteristics for USB DP/DM

- **Accepted cable characteristics:**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ZO	Differential cable impedance (High-/full- speed)	-	76.5	90	103.5	Ω

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ZCM	Common mode cable impedance (High-/full- speed)	-	21	30	39	Ω
TSKEW	Cable skew	-	-	-	100	ps
CUC	Unmated contact capacitance	-	-	-	2	pF

Table 3-15 Electrical Characteristics for US Accepted Cable

■ Reliability characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
HBM1	ESD Human Body Mode	-	-	-	±2.0	kV
MM	ESD Machine Mode	-	-	-	±100	V
CDM	ESD Charged Device Mode	-	-	-	±250	V
VLATCH_33	Latch-up trigger voltage	VCC33A domain	-	-	5.4	V
VLATCH_18	Latch-up trigger voltage	VCC18A domain	-	-	2.97	V
VLATCH_09	Latch-up trigger voltage	VCC09A domain	-	-	1.35	V
ILATCH	Latch-up trigger current	-	-	-	±200	mA

Table 3-16 Reliability Characteristics

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4. Design Recommendation

The following diagram provides the PCB architecture of the EVB design for your reference.

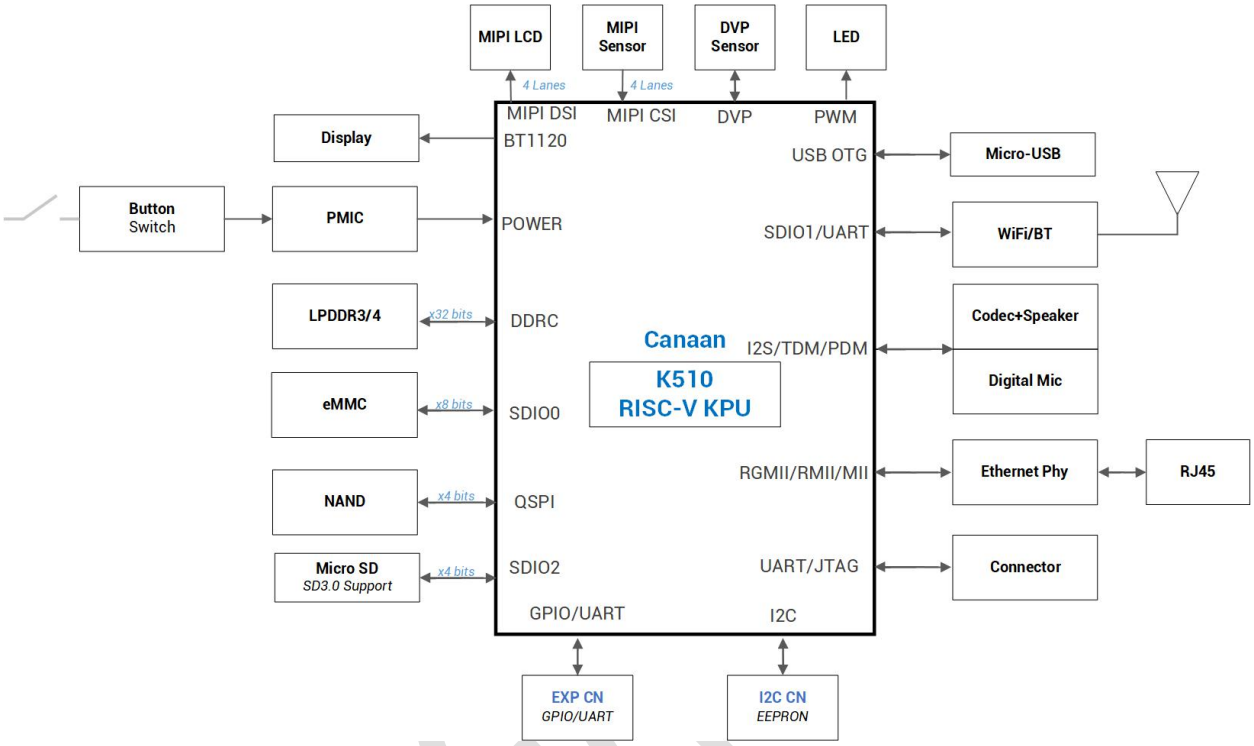

Figure 4-1 PCB Architecture Diagram

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Terms/Abbreviations

Term/Abbreviation	Description/Full Name
OTP	One Time Program
PUF	Physical Un-cloned Function
AES	Advanced Encryption Standard
DDR	Double Data Rate
eMMC	Embedded Multi-Media Card
GNNE	General Neural Network Engine
KPU	Knowledge Processing Unit
UART	Universal Asynchronous Receiver/Transmitter
CSI	Camera Serial Interface
DSI	Display Serial Interface
PPI	Parallel Peripheral Interface
DPI	Display Pixel Interface
FPU	Float Point Unit
MII	Media Independent Interface
RGMII	Reduced Gigabit Media Independent Interface
I2S	Inter-IC Sound
GPIO	General Purpose I/O
OTG	On-the-Go

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Term/Abbreviation	Description/Full Name
SD	Security Digital
MMC/eMMC	Multi-media Card/Embedded Multi-media Card
SDMA	System Direct Memory Access
PDMA	Peripheral Direct Memory Access
VAD	Voice Activity Detection
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
BIST	Built-in Self Test
BSR	Boundary-scan Register

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