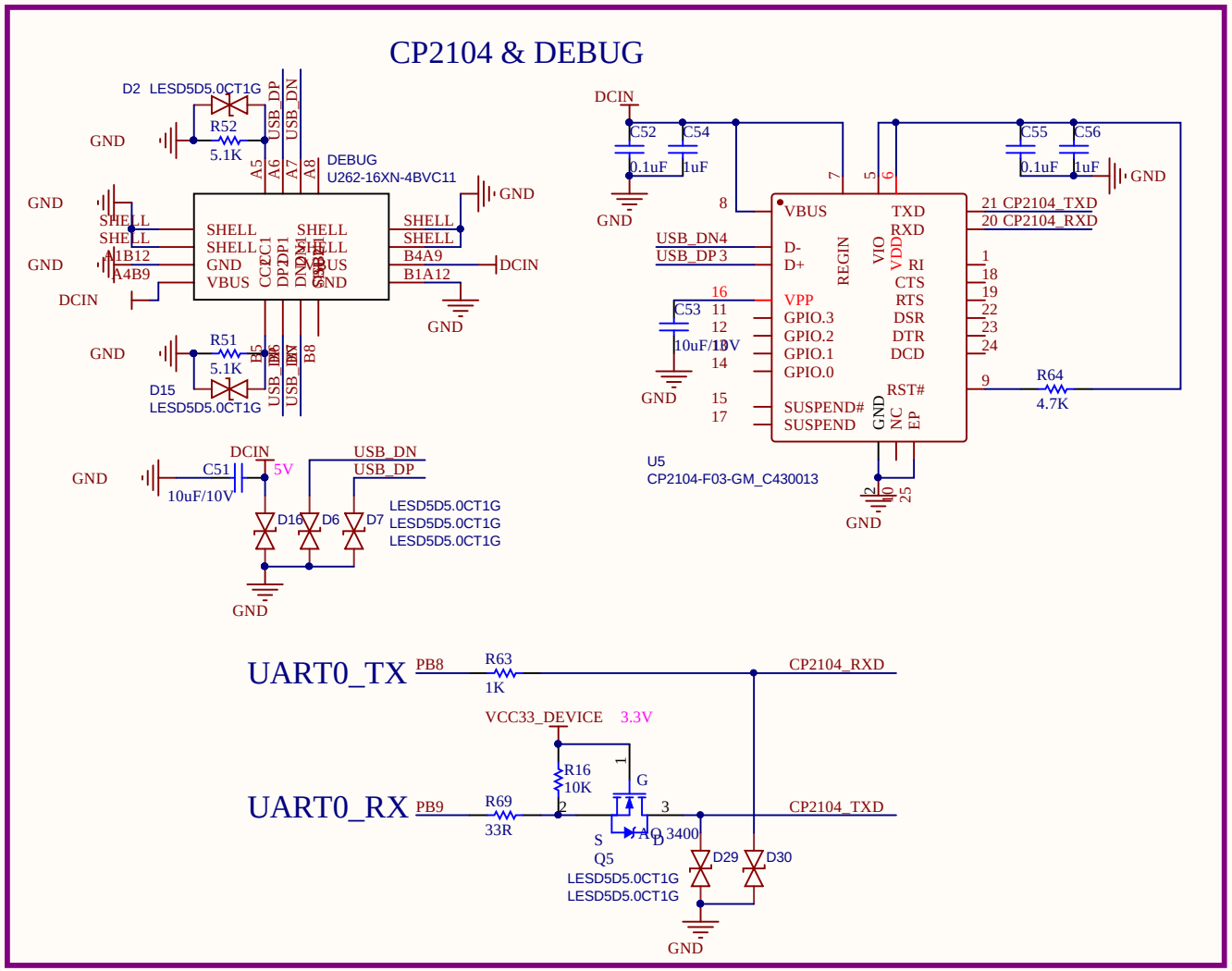
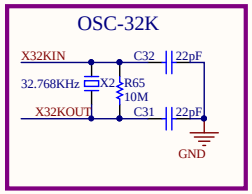
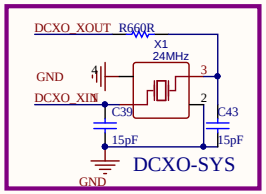
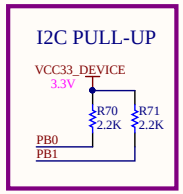
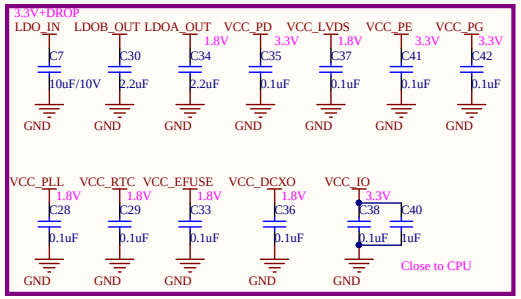


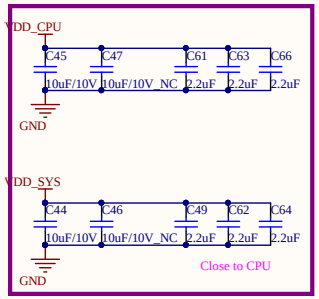
Title		
Size A4	Number	Revision
Date: 2022/3/9	Sheet of	
File: H:\东山-哪吒STU开发板\..\CP2104.SchDoc	Drawn By:	

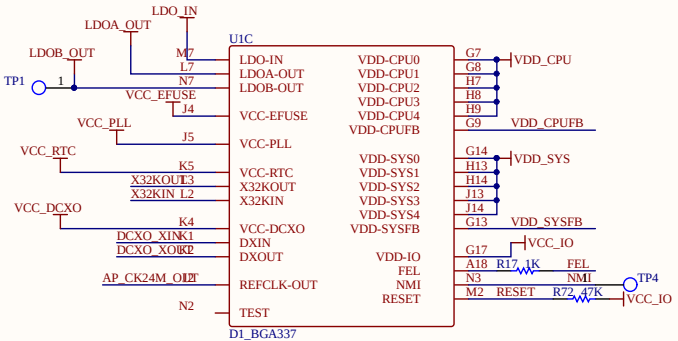


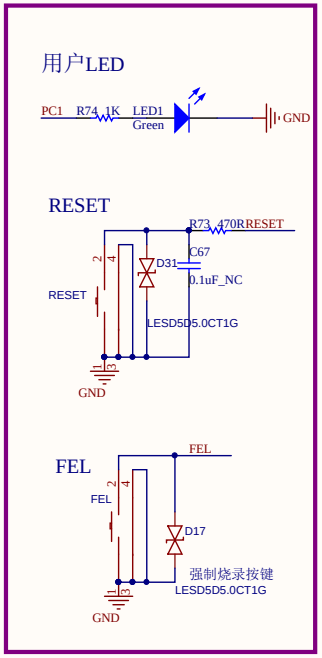


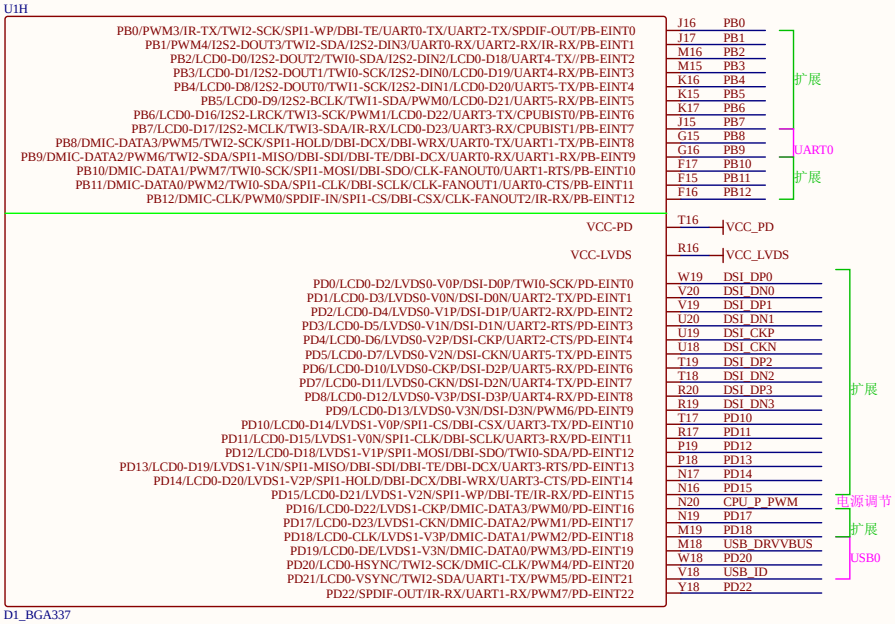


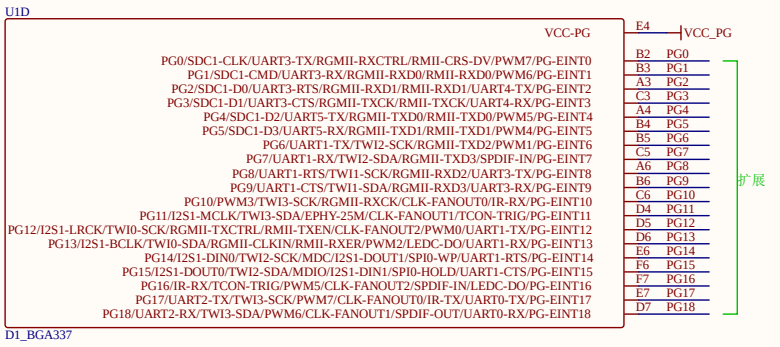




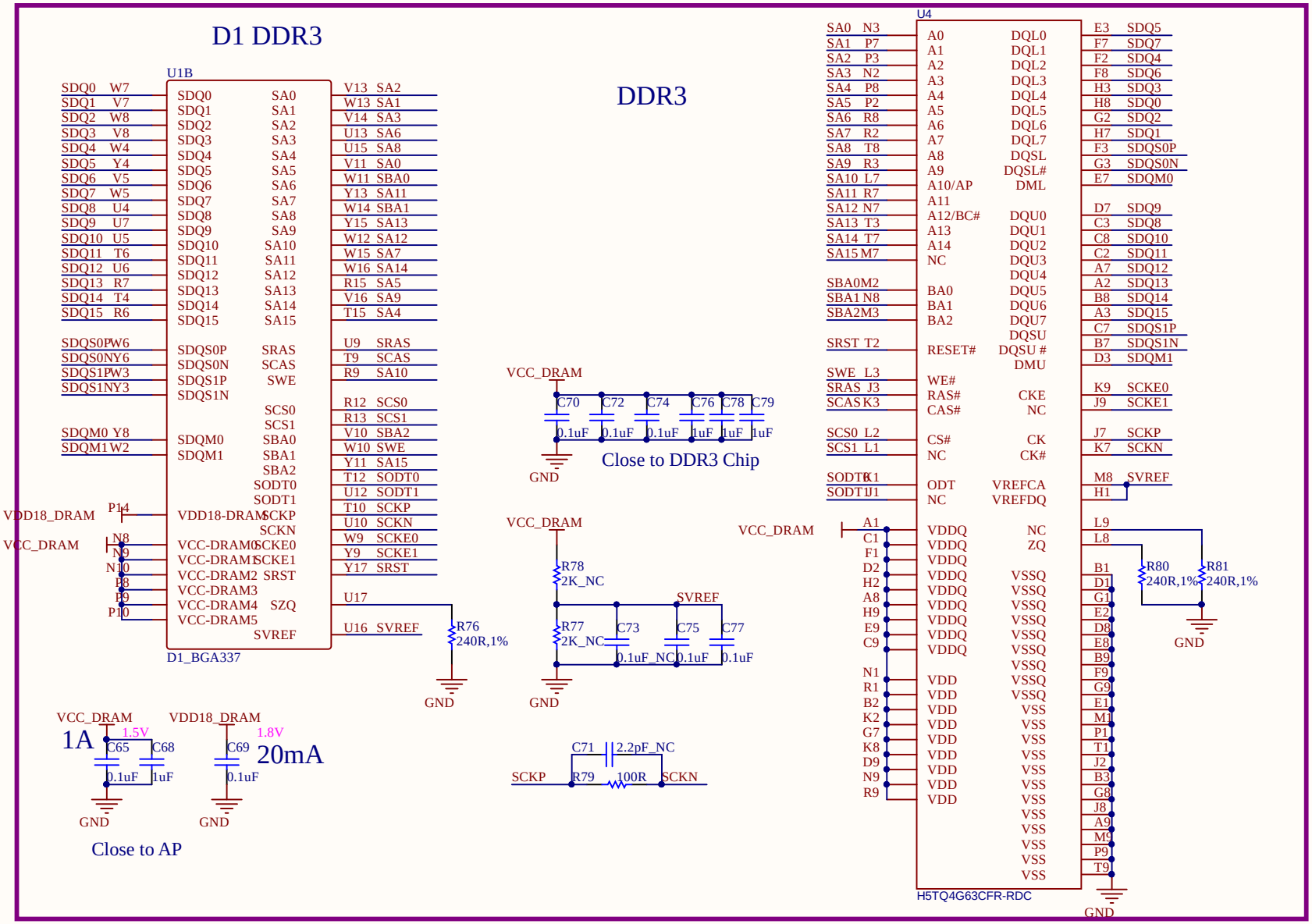






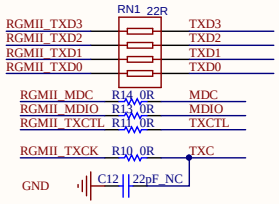


Title		
Size A3	Number	Revision
Date: 2022/3/9	Sheet of	
File: H:\东山-哪吒STU开发板\...\D1_CORE.SchDoc	Drawn By:	



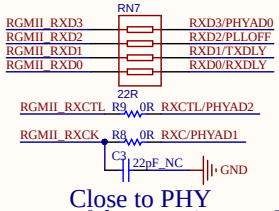
Title		
Size: A4	Number	Revision
Date: 2022/3/9		Sheet of
File: H:\东山-哪吒STU开发板\..\DDR3.SchDoc		Drawn By:

RGMII TX Filter Network

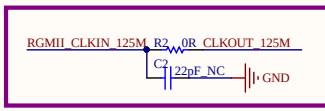


Close to SOC
Reserved for EMI.(optional)

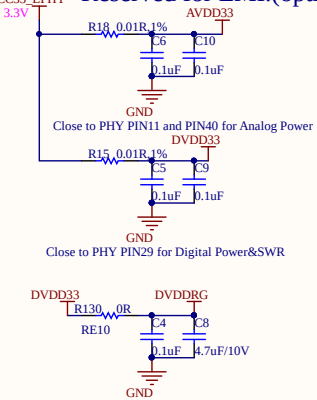
RGMII RX Filter Network



Close to PHY
Reserved for EMI.(optional)

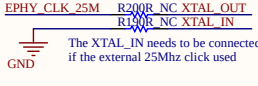


Reserved for EMI.(optional)

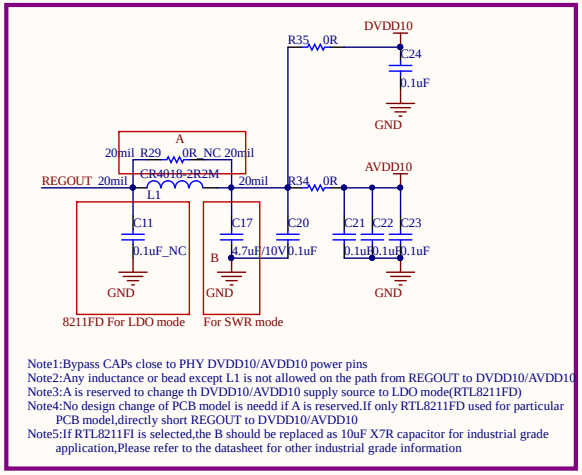


Note1:RE10 is not needed for only 3.3v RGMII application, and DVDDRG can be connected directly to DVDD33
Note2:DVDDRG must be short(or RE10 be mounted) to DVDD33 if the external RGMII 3.3V is selected
Note3:RE10 must be removed if the internal or external 2.5V/1.8V/1.5V RGMII is selected
Note4:CAPs must be closed to pin28 for EMI consideration

External Clock Case



The XTAL_IN needs to be connected to GND if the external 25Mhz click used

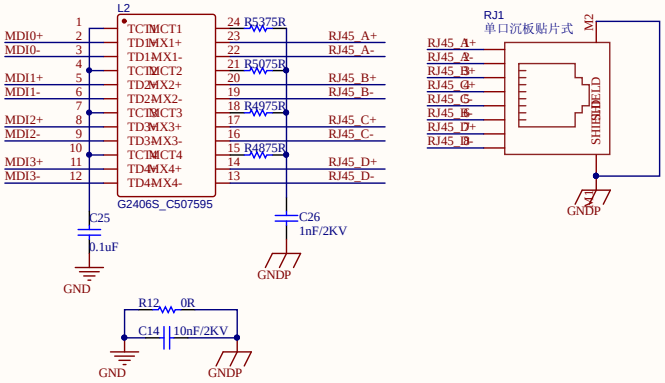


Note1:Bypass CAPs close to PHY DVDD10/AVDD10 power pins
Note2:Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10
Note3:A is reserved to change th DVDD10/AVDD10 supply source to LDO mode(RTL8211FD)
Note4:No design change of PCB model is needd if A is reserved.If only RTL8211FD used for particular PCB model,directly short REGOUT to DVDD10/AVDD10
Note5:If RTL8211FI is selected,the B should be replaced as 10uF X7R capacitor for industrial grade application,Please refer to the datasheet for other industrial grade information

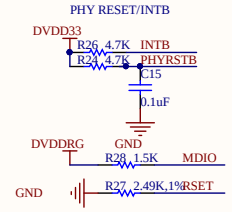
Tranformer

Differential pairs
Z0=100 OHM

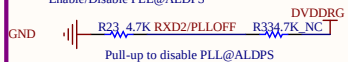
RJ45



PHY RESET/INTB

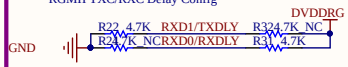


Enable/Disable PLL@ALDPS



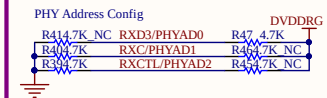
Pull-up to disable PLL@ALDPS

RGMII TXC/RXC Delay Config



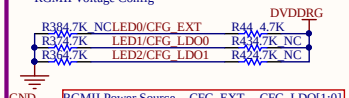
Pull-up for additional 2ns delay to TXC/RXC for data latching

PHY Address Config



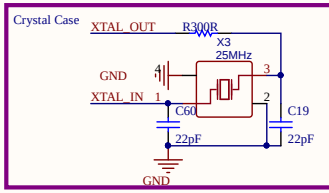
PHY Address	PHY AD[2:0]
0	3'b000
1(default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

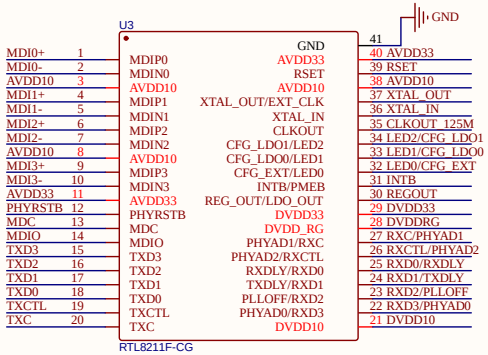
RGMII Voltage Config



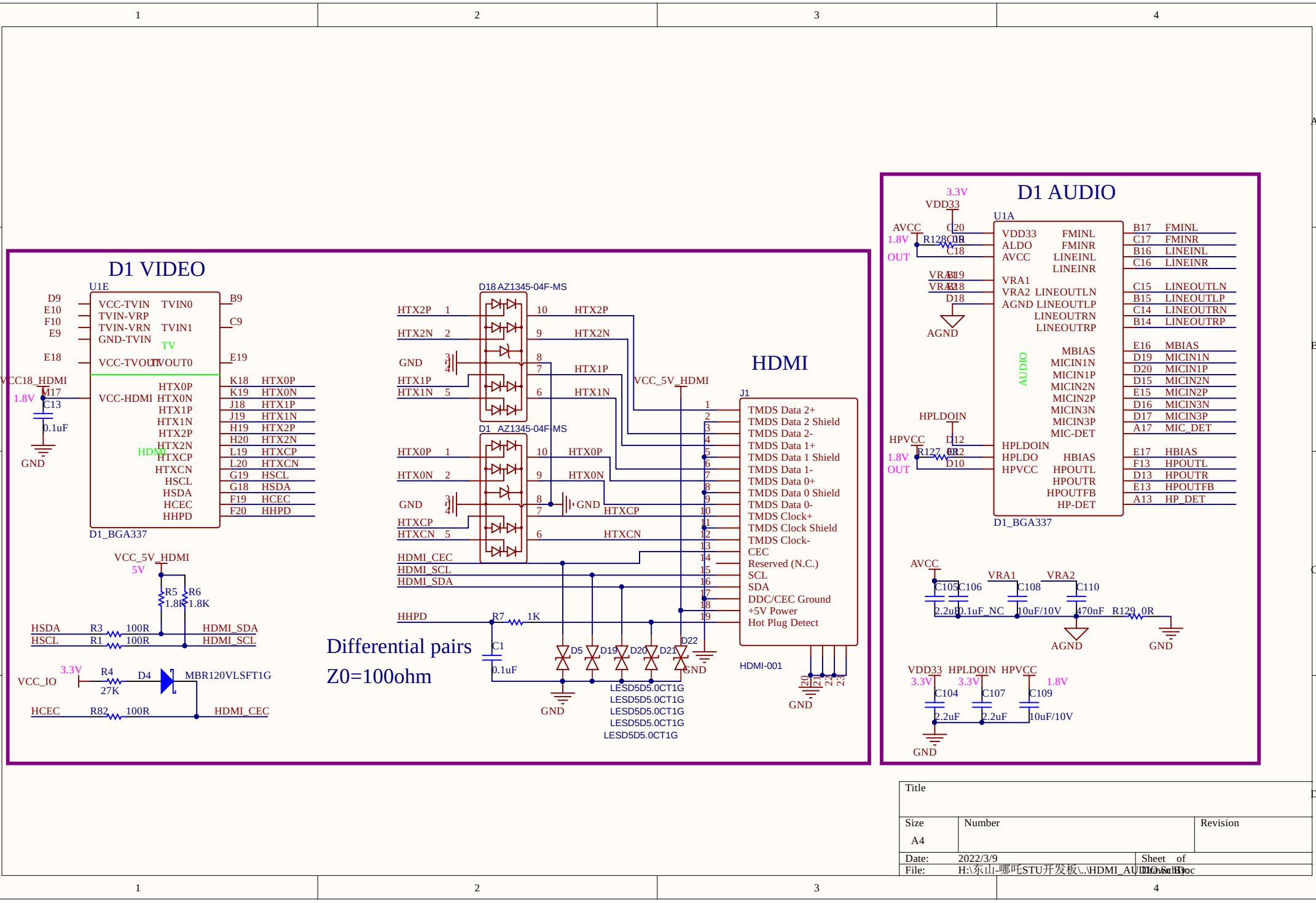
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V(default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

Crystal Case

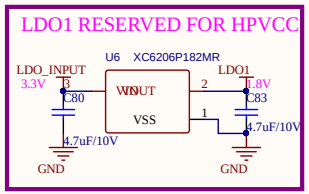


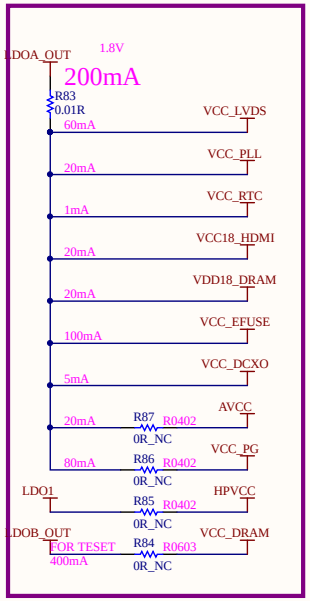


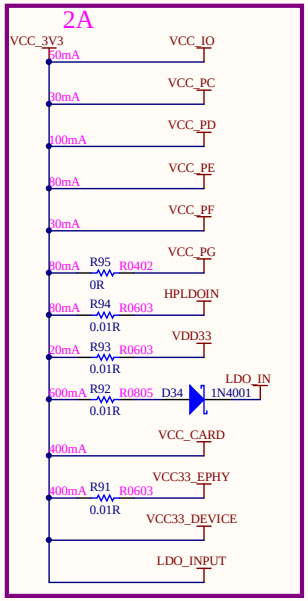
Title			
Size A3	Number		Revision
Date: 2022/3/9		Sheet of	
File: H:\东山-哪吒STU开发板\..\ETHERNET.SchDoc		Drawn By:	

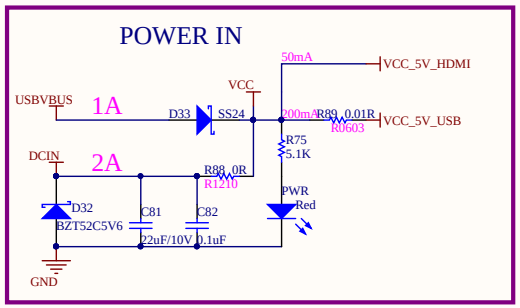


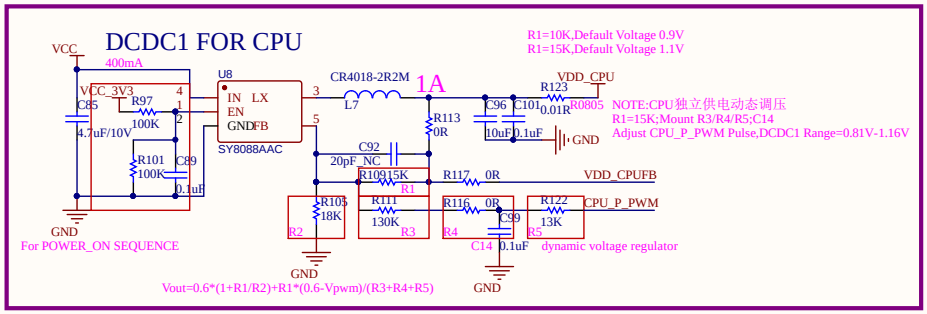
Title		
Size A4	Number	Revision
Date: 2022/3/9		Sheet of
File: H:\东山-哪吒STU开发板\..\HDMI_AUDIO.SchDoc		Drawn By:

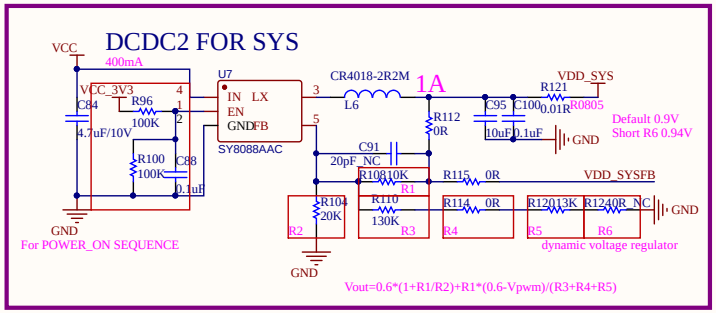


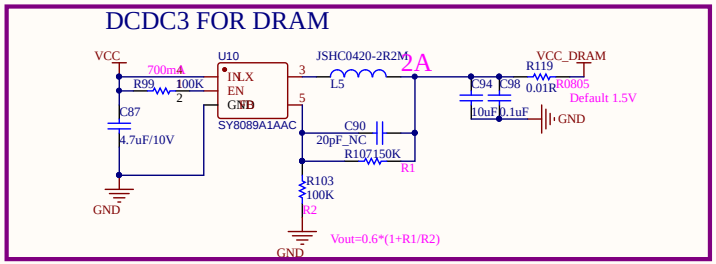


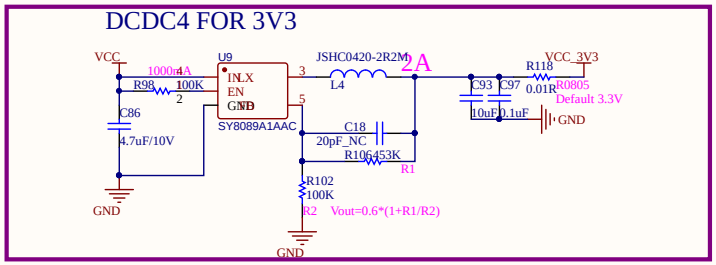




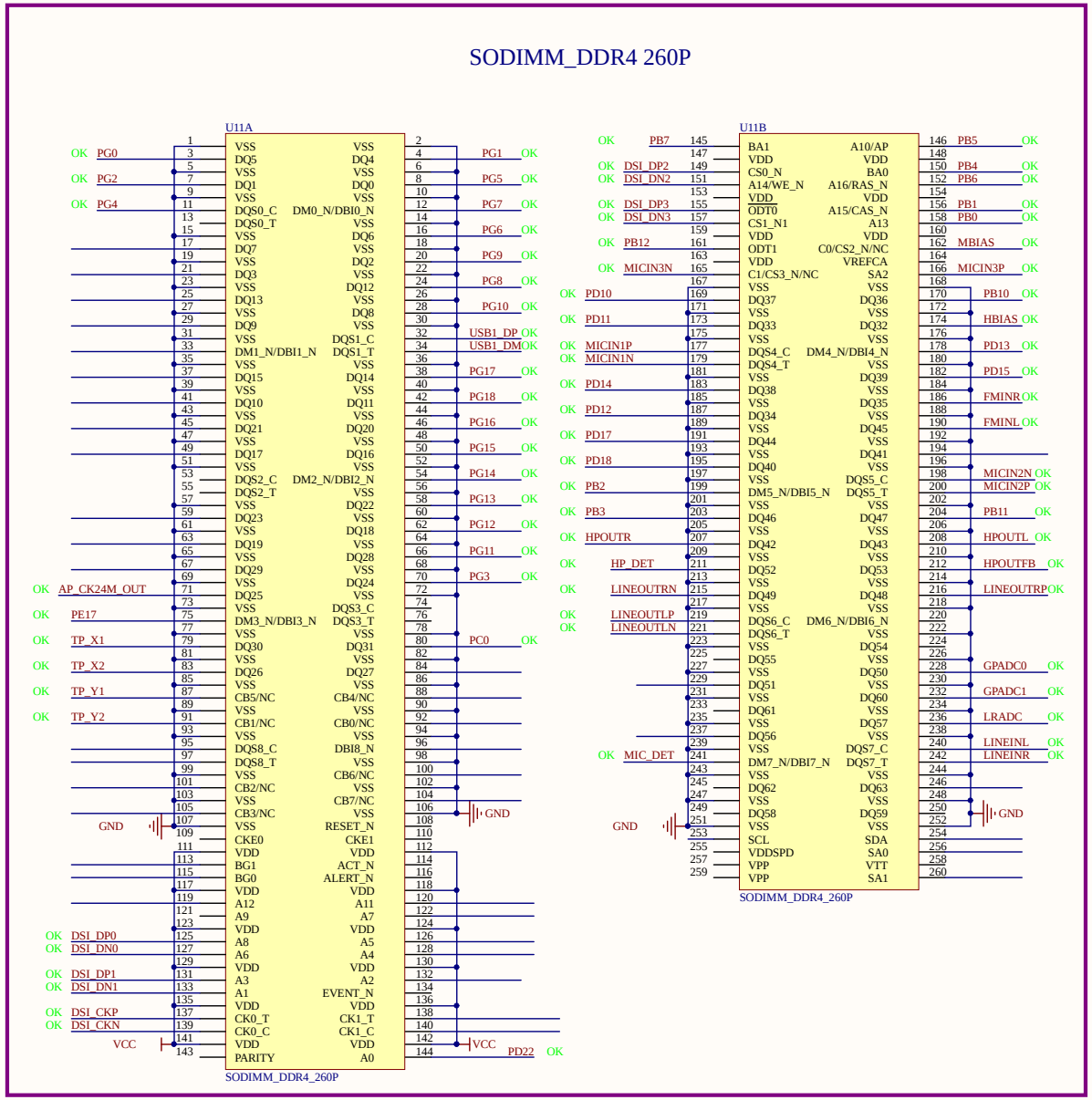




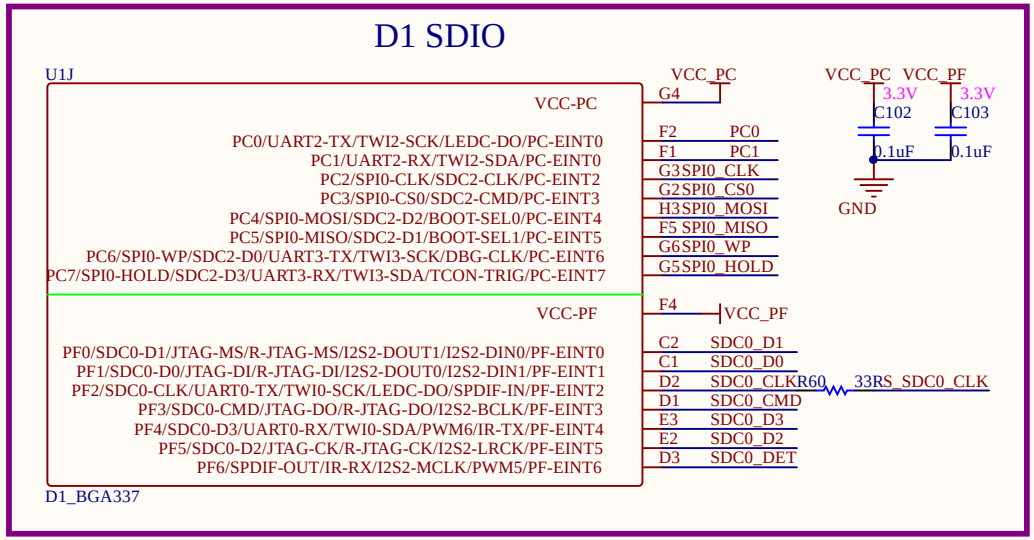


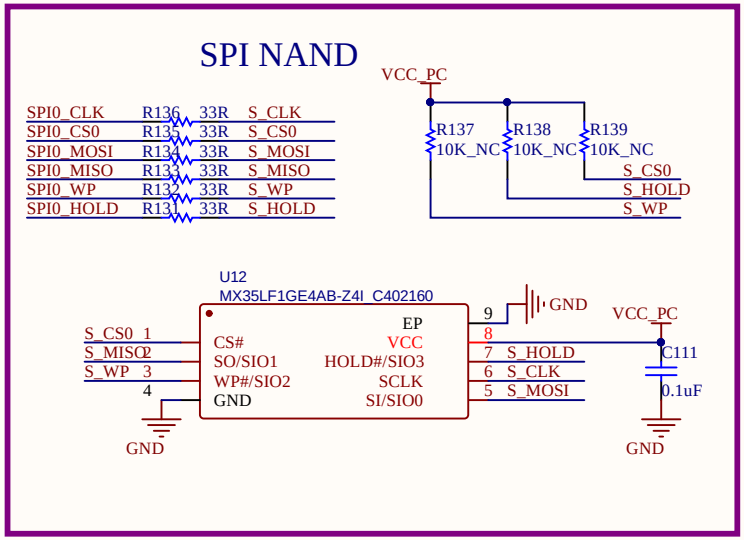


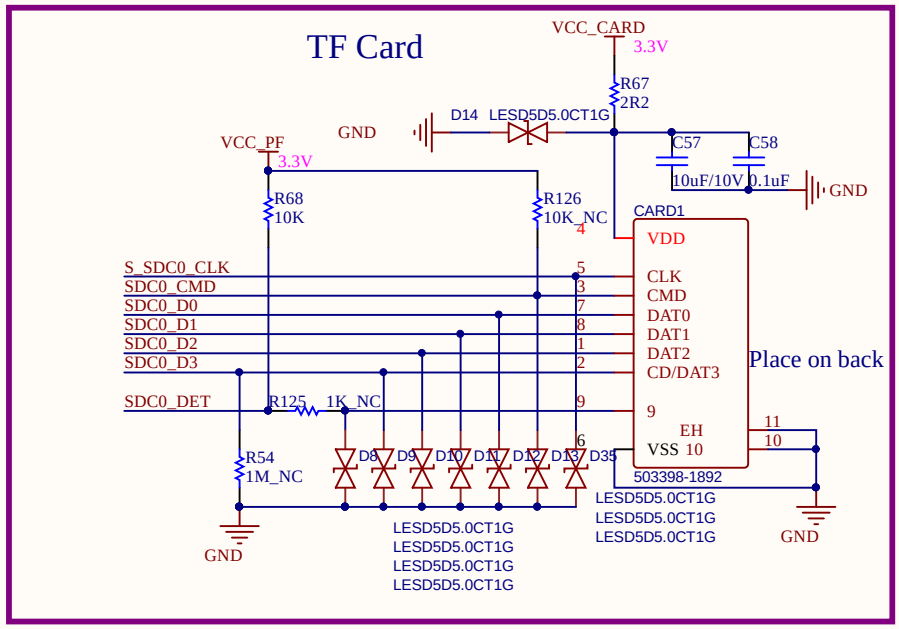
Title		
Size A3	Number	Revision
Date: 2022/3/9	Sheet of	
File: H:\东山-哪吒STU开发板\...\POWER.SchDoc	Drawn By:	



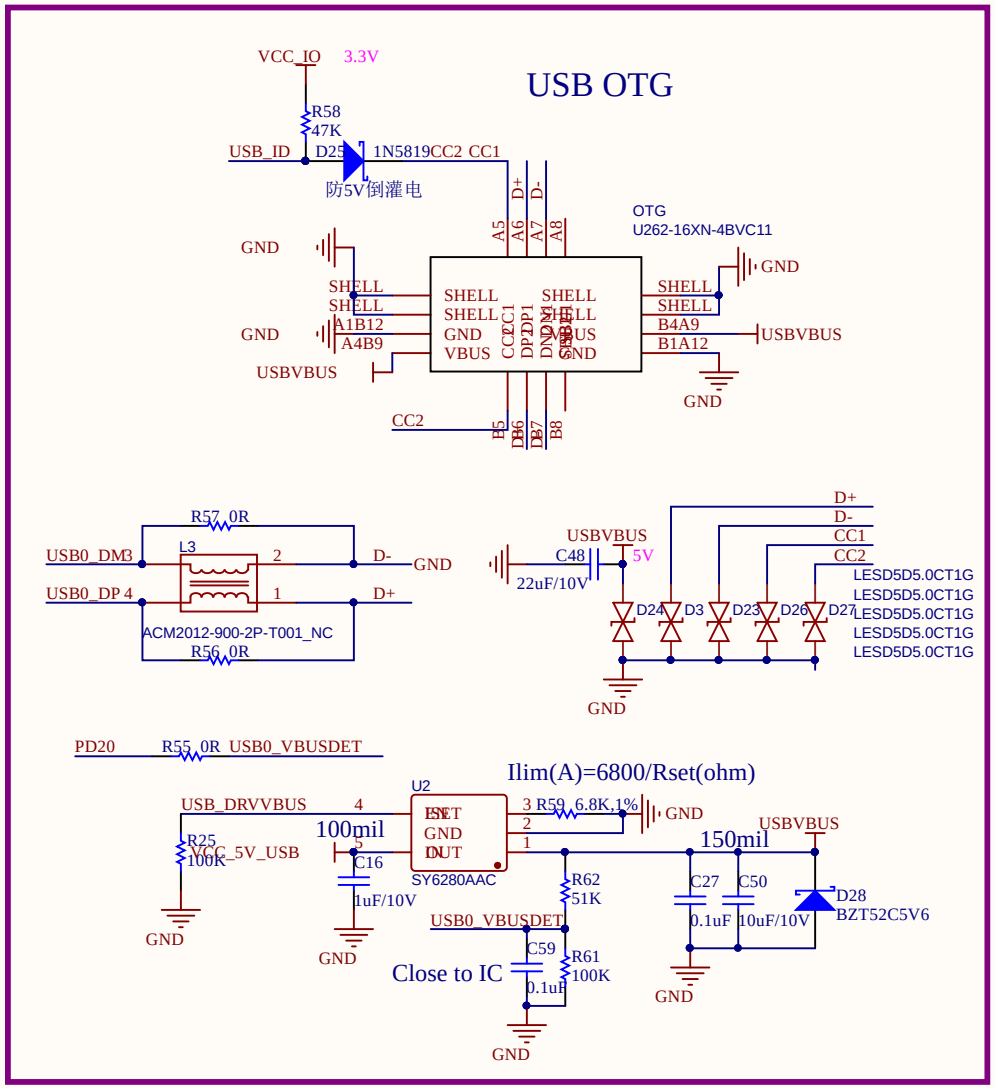
Title		
Size A3	Number	Revision
Date: 2022/3/9	Sheet of	
File: H:\东山-哪吒STU开发板\...\SODIMM_DDR4_260P.SchDoc	Drawn By:	

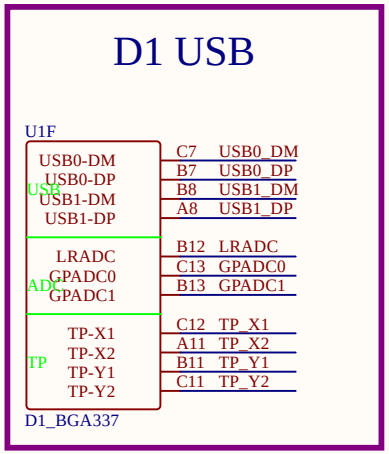


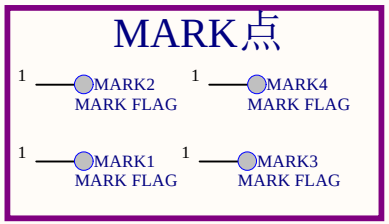


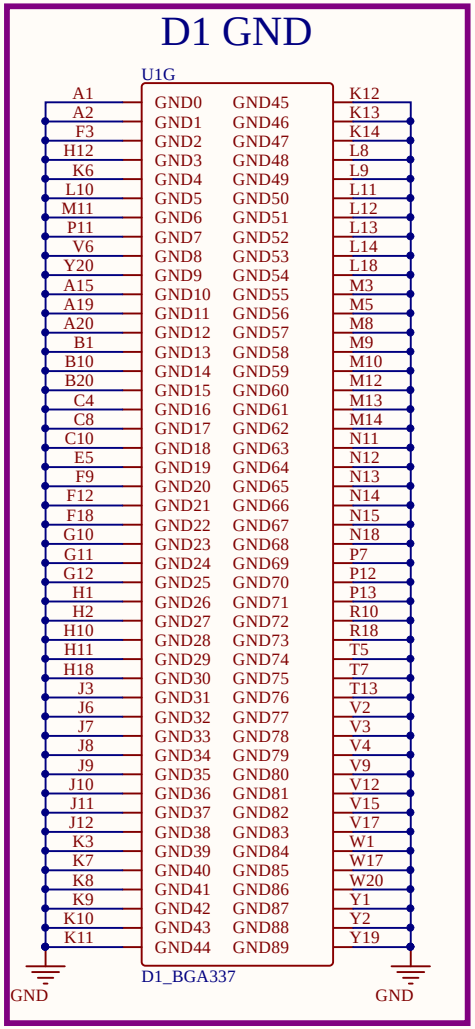


Title		
Size A4	Number	Revision
Date: 2022/3/9		Sheet of
File: H:\东山-哪吒STU开发板\..\TF_SPI_NAND.SchDoc		Drawn By:









Title		
Size A4	Number	Revision
Date: 2022/3/9		Sheet of
File: H:\东山-哪吒STU开发板\..\USB.SchDoc		Drawn By: