深圳信显光电科技有限公司

Shenzhen Sincere Optoerec tronic technology Co.Ltd.

产 品 承 认 书
SPECIFICATION FOR APPROVAL

CUSTOMER MODEL NO.	
WEITAI MODEL NO.	SM068-102A4
TYPE	LCD MODULE, 480*(RGB)1280

WEITAI			**CUSTOMER**
PREPARED	**CHECKED**	**APPROVED**	**APPROVED**

深圳信显光电科技有限公司

地址：**深圳市宝安区石岩料坑喜源通工业园 8 栋 6 楼**

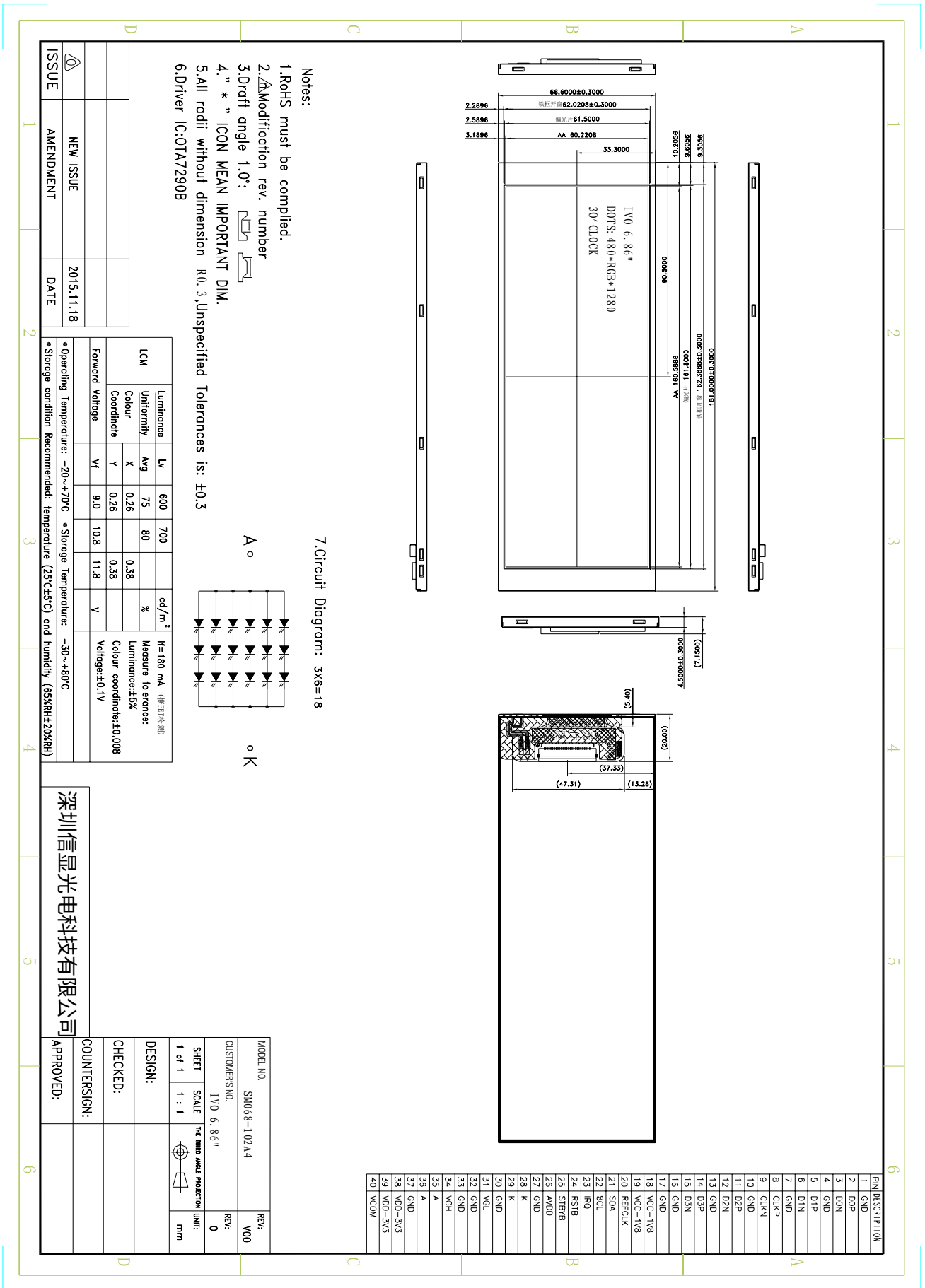
本规格承认书请确认签章后回传一份

变更记录表

变更序号 Change No.	日期 Date	内容及理由 Subject And Reason	版本号 Version No.	负责人 Responser
1	2015.12.14	首次发行	A0	

目　　录

四、模组成品图纸



Notes:

1.RoHS must be complied.

2.△Modification rev. number

3.Draft angle 1.0°:

4." * " ICON MEAN IMPORTANT DIM.

5.All radii without dimension R0.3,Unspecified Tolerances is: ±0.3

6.Driver IC:OTA7290B

7.Circuit Diagram: 3X6=18

ISSUE	AMENDMENT	DATE
0	NEW ISSUE	2015.11.18

LCM						
Luminance		Lv	600	700		cd/m²
Uniformity		Avg	75	80		%
Colour Coordinate		X	0.26		0.38	If=180 mA (裸屏环境测) Measure tolerance: Luminance:±5% Colour coordinate:±0.008
		Y	0.26		0.38	
Forward Voltage		Vf	9.0	10.8	11.8	V Voltage:±0.1V

- Operating Temperature: -20~+70°C
- Storage Temperature: -30~+80°C
- Storage condition Recommended: temperature (25°C±5°C) and humidity (65%RH±20%RH)

MODEL NO.:	SM068-102A4
CUSTOMER'S NO.:	IVO 6.86"
REV:	0
SCALE	1 : 1
SHEET	1 of 1
UNIT:	mm
DESIGN:	
CHECKED:	
APPROVED:	
COUNTERSIGN:	

深圳信显光电科技有限公司

五、玻璃参数

1 General Descriptions

1.1 Introduction

SM068-102A4 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) Single Chip and Sub Chips that uses amorphous silicon TFT as a switching device. This TFT LCD panel has a 6.8 inch diagonally measured active display area with WXGA resolution (480 horizontal by 1280 vertical pixels array).

1.2 Features

- 6.8" TFT-LCD Panel
- Supported WXGA Resolution
- Compatible with RoHS Standard

1.3 General Characteristics

Table 1 General Characteristics

Item	Specification	Unit	Note
Outline Dimension (H x V x D)	63.4208 x169.0888x 1.0	mm	Single Chip
Active Area (H x V)	60.2208 x 160.5888	mm	Single Chip
Number of Pixels (H x V)	480 x1280	-	Single Chip
Pixel Size (H x V)	0.1254 x0.1254	mm	Single Chip
Pixel Arrangement	RGB Stripe	mm	Single Chip
Display Type	Transmissive	-	-
Display Mode	Normally White	-	-
Cell Thickness	CF: 0.50±0.05	mm	-
	TFT: 0.50±0.05		
Driver IC(Recommendation)	OTA7290B	-	-
Weight	25.2 (Typ.)	g	Single Chip
	537.7(Typ.)	g	20 Sub Chips

3 Electrical Specifacations

Table 3 Electrical Specifications

No.	Item	Min	Typ	Max	Unit
1	Vcom voltage	3.2	4.2	5.2	V
2	Frame Rate	55	60	65	Hz
3	VGH voltage	17	19	21	V
4	VGL voltage	-10	-8	-6	V
5	AVDD	10	12	14	V
6	VDD	2.7	3.3	3.6	V
A	VCC		1.8		V

敬告客户：

样机电流测试参考：

VCOM为4.2V时电流为1.15mA；

VGH为18V时电流为4.5mA；

VGL为-8V时电流为-1.4mA；

AVDD为9.7V时电流为10.5mA；

VDD为3.3V时电流为1.0mA；

VCC为1.8V时电流为16mA；

Note (1) VGH is TFT gate operating voltage
Note (2) VGL is TFT gate operating voltage
Note (3) Vcom must be adjusted to optimize display quality: Crosstalk, Contrast Ratio etc.
Note (4) Environmental condition: 25±5 ºC
Note (5) We just kindly recommend the setting-voltage as the reference value. In order to get the
optimized display quality, the setting-voltage should be changed as based on customer's developing
condition.

2 Absolute Maximum Ratings

Table 2 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
LC Operating Voltage (Ta = 25℃)	V_{OP}	-5.5	5.5	V	(1),(2), (3)
Operating Temperature	T_{OP}	-20	80	℃	
Operating Humidity	H_{OP}	10	80	%RH	
Storage Temperature	T_{ST}	-40	80	℃	
Storage Humidity	H_{ST}	10	90	%RH	

Note (1) Liquid Crystal driving voltage due to the characteristics of LC Material, this voltage varies with environmental temperature.

Note (2) Maximum Wet-Bulb should be 39 ℃. No condensation of water

Note (3) When the LCD Panel is working Please make sure to keep the temperature of LCD panel is less than 80℃

4 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 4 Optical Characteristics

Item	Conditions		Min.	Typ.	Max.	Unit	Note
Transmittance	-		3.81	4.24	-	%	(1),(5),(6),(8),(9)
Contrast Ratio	Center		800	1000	-	-	(1),(3),(7),(8),(9)
Response Time	Rising + Falling		-	20	TBD	ms	(1),(4),(7),(8),(9)
CF Color Chromaticity (CIE1931)	Red x		Typ. -0.03	0.648	Typ. +0.03	-	Under C-light
	Red y			0.328		-	
	Green x			0.277		-	
	Green y			0.556		-	
	Blue x			0.138		-	
	Blue y			0.128		-	
	White x			0.295		-	
	White y			0.323		-	
NTSC	CIE1931		(55)	60	-	%	(1),(6),(8),(9)
Viewing Angle （CR>10）	Horizontal	θ_{x+}	-	60	-	degree	(1),(2),(7),(8),(9) Viewing Angle base on using EWV Polarizer Reference only
		θ_{x-}	-	70	-		
	Vertical	θ_{y+}	-	70	-		
		θ_{y-}	-	70	-		

六、IC 时序

8.3.2. MIPI DC Characteristics

HS Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Operation Voltage	VDD	1.5-10%	1.5	1.5+10%	mV	
Differential Input Voltage	|VID|	70	200	260	mV	
Common Mode Voltage	$V_{CMRX(DC)}$	70	-	330	mV	
Differential Input High Threshold Voltage	VTH	-	-	70	mV	
Differential Input Low Threshold Voltage	VTL	-70	-	-	mV	
Singled-ended input high voltage	V_{IHHS}	-	-	460	mV	
Singled-ended input low voltage	V_{ILHS}	-40	-	-	mV	
Singled-ended threshold for HS termination enable	$V_{TERM-EN}$	-	-	450	mV	
Differential input impedance	Z_{ID}	80	100	125	ohm	
Pin leakage current	I_{LEAK}	-10	-	10	uA	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	
Common-mode interference 50MHz - 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	
Common-mode termination	C_{CM}	-	-	60	pF	
Embedded Termination	R_T	90	100	110	ohm	2bits RT_SEL[1: 0] for termination resistor selection 00 → 200ohm 10 , 01→ 150ohm 11 → 100ohm (default) 1bit ERMR_EN for termination resistor enable TERMR_EN=0, termr disable R=(OPEN) TERMR_EN=1, termr enable

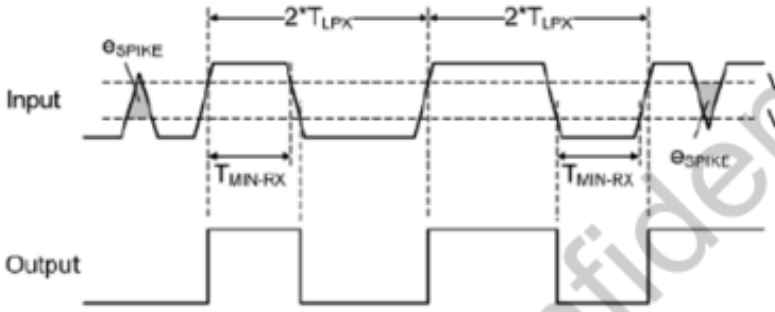
Note:

(1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

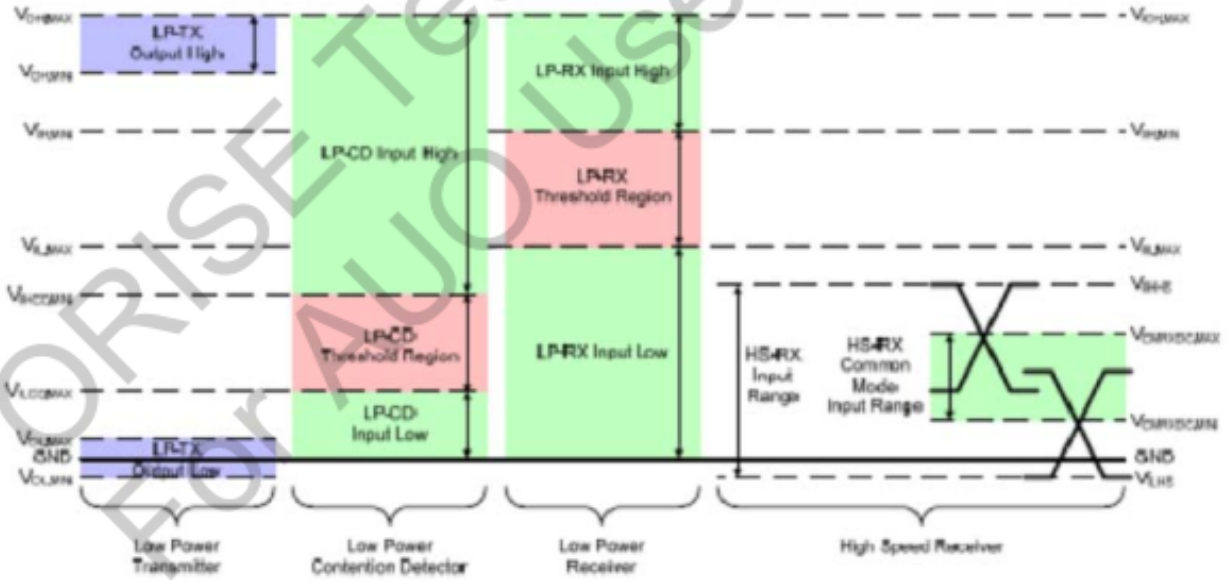
LP Receiver DC Specification

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Input hysteresis	V_{HYST}	25	-	-	mV	



Line Contention Detection

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	VILCD	-	-	200	mV	



Input Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Pin signal voltage range	V_{PIN}	-50		1350	mV	
Pin leakage current	I_{LEAK}	-10		10	uA	
Ground shift	V_{GNDSH}	-50		50	mV	
Transient pin voltage level	$V_{PIN(absmax)}$	-0.15		1.45	V	
Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$	$TV_{PIN(absmax)}$			20	ns	

Note:

(1) When the pad voltage is in the signal voltage range from VGNDSH, MIN to VOH + VGNDSH, MAX and the Lane Module is in LP receive mode.

(2) The voltage overshoot and undershoot beyond the VPIN is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the VPIN range.

(3) This value includes ground shift.

8.4. AC Characteristics

8.4.1. System AC Characteristics

(VDD=3.3V, AVDD=12V, VSS=VSSA=0V, TA=-20 to +85℃)

Parameter	Symbol	MIN.	Typ.	MAX.	UNIT	Conditions
VDD Power On Slew rate	T	-	-	20	ms	From VSS to 90% VDD
RSTB pulse width	T	10	-	-	us	

8.4.2. MIPI AC Chrematistics

HS Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Bandwidth per lane	-	-	-	1000	Mbps	Bandwidth selected by register 'speedup' Speedup=0 → Max=550Mbps Speedup=1→ Max=1000Mbps
Operation frequency	-	-	-	500	MHz	
UI instantaneous	UI_{INST}	1	-	12.5	ns	1
Data to Clock Skew	Tskew	-0.15	-	0.15	UI_{INST}	
Inter-lane static skew	Tskew-lane	-	-	$UI_{INST}/50$	UI_{INST}	
Data to Clock Setup Time	T_{SETUP}	0.25	-	-	UI_{INST}	2
Data to Clock Hold Time	T_{HOLD}	0.25	-	-	UI_{INST}	
Common-mode interference beyond 450MHz	$\Delta V_{CMRX(HF)}$	-	-	100	mV	4
Common-mode interference 50MHz- 450MHz	$\Delta V_{CMRX(LF)}$	-50	-	50	mV	3,6
Common-mode termination	C_{CM}	-	-	60	pF	5

Note:

(1) Total silicon and package delay budget of 0.3*UINST

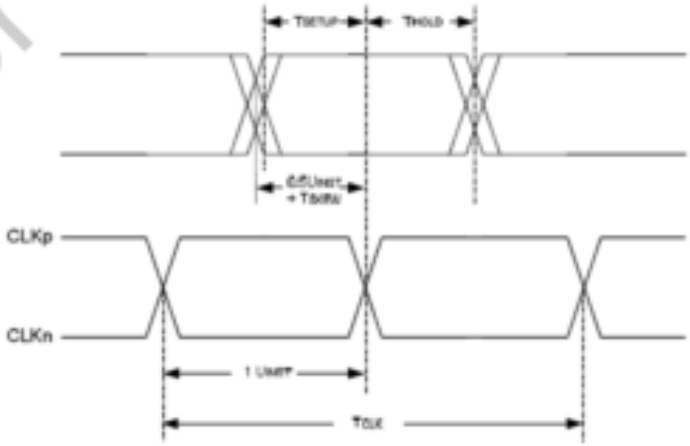
(2) Total setup and hold window for receiver of 0.3*UINST

(3) Excluding 'static' ground shift of 50mV

(4) =VCMRX (HF) is the peak amplitude of a sine wave superimposed on the receiver input

(5) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

(6) Voltage difference compared to the DC average common-mode potential.



LP Receiver AC Timing Characteristics

Parameter	Symbol	Rating			Unit	Note
		Min	Typ	Max		
Input pulse rejection	e_{SPIKE}	-	-	300	V·ps	1,2,3
Minimum pulse width response	T_{MIN-RX}	20	-	-	ns	
Peak interference amplitude	V_{INT}	-	-	200	mV	
Interference frequency	f_{INT}	450	-	-	MHz	
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	
Input Hysteresis	V_{HYST}	25	-	-	mV	
Logic 1 contention threshold	V_{IHCD}	450	-	-	mV	
Logic 0 contention threshold	V_{ILCD}	-	-	200	mV	

Note:

(1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1state.

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.