Artmem eMMC5.1 Datasheet

AT70B16G4T06F

Revision 0.1

Jun.10, 2021

Revision History

Version	Date	Editor	History
V0.1	2021-6-10		Initial release.

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change at any time without notice, as further product development and data characterization sometimes occur.

Contents

1. Product Overview

1.1. Introduction

Artmem eMMC product is a high quality and cost advantage embedded storage solution and compatible with JEDEC standard eMMC5.1 specification. Its strong ECC engine significantly improves error correction enabling longer device lifetime and an increased ability to handle higher raw bit error rate.

The Artmem eMMC product consists of NAND flash and an eMMC controller. The eMMC controller and software directly manage NAND flash, including ECC, wear-leveling, bad block management, garbage collection and performance optimization, and manage interface protocols. This architecture insulates any revision of NAND flash from the eMMC Host, makes the eMMC device easy to integrate and accelerates time-to-market.

1.2. Feature Overview

eMMC feature overview:

- eMMC 5.1 specification compatibility
  - Backward compatible to eMMC 4.41/4.51/5.0
- Bus mode
  - Data bus width: 1 bit (default), 4 bits, 8 bits
  - Data transfer rate: up to 400MB/s (HS400)
  - Clock frequency : 0~200MHz
- Operating voltage range
  - V_{CC}: 2.7 - 3.6V
  - V_{CCQ} : 1.7 - 1.95V or 2.7 - 3.6V
- Support Hardware ECC engine
- Support auto power saving mode
- Preventing from sudden-power-off
- Support features defined in JEDEC standard
  - RPMB
  - Boot partition
  - Write protection
  - Erase, discard, trim, sanitize
  - HPI
  - Background operations
  - Device health report
  - Field firmware update(FFU)
  - Sleep / awake
  - Packed command
- Temperature range

Part Number	Operation	Storage without Operation
AT70B16G4T06F	-25°C ~ 85°C	-40°C ~ 85°C

1.3. Product List

Table 1.3- 1. Product List

Density	Part Number	NAND Flash Type	User Density (MB)	Package Size (mm)	Pin Configuration
16 GB	AT70B16G4T06F	128Gb x 1	14,912	11.5x13x0.92	153 TFBGA

2. Product Specification

2.1. Partition Size

2.1.1. Factory Configuration

The device initially consists of two Boot Partitions, RPMB Partition and User Data Area. Both Boot and RPMB area have fixed size of area and can not be adjusted.

Table 2.1- 1. Partition Size

Density	Boot Partition 1 (KB)	Boot Partition 2 (KB)	RPMB (KB)	User Data Area	
				Percent	Size (MB)
16 GB	4096	4096	4096	91%	14,912

2.1.2. Partition Management

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition with independent address spaces, starting from logical address 0x0000000. Each of the General Purpose Area Partitions and a section of User Data Area partition can be configured as enhanced partition. These partition management operations are one-time programmable.

The enhanced partitions are true SLC mode partition. When customer set some portion as enhanced partitions in User Data Area, these partitions occupy double(MLC)/triple(TLC) size of the original set-up size. If set 1MB for enhanced mode, total 2MB(MLC)/3MB(TLC) user data area is needed to generate 1MB enhanced area.

Table 2.1- 2. Max Enhanced Partition Size

Density	Max. Enhanced Partition Size (MB)
16 GB	4,968

2.2. Power Consumption

2.2.1. Standby State

Table 2.2- 1. Power consumption in auto power saving mode and standby state

Density	I_{CCQ} (uA)		I_{CC} (uA)	
	25°C(Typ.)	85°C	25°C(Typ.)	85°C
16 GB	100	450	TBD	TBD

Note:

1. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.
2. In Standby Power mode, V_{CCQ} & V_{CC} power supply is switched on. No data transaction period before entering sleep status, no clock. V_{CCQ} = 1.8V & V_{CC} = 3.3V. Not 100% tested.

2.2.2. Sleep State

Table 2.2- 2. Power consumption in sleep state

Density	I_{CCQ} (uA)		I_{CC} (uA)
	25°C(Typ.)	85°C	
16 GB	100	450	0

Note:

1. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.
2. In Sleep state, triggered by CMD5, V_{CC} power supply is switched off (V_{CCQ} on). V_{CCQ} = 1.8V & V_{CC} = 0V. Not 100% tested.
3. In auto power saving mode, NAND power V_{CC} can not be switched off. However in sleep mode V_{CC} can be switched off. If NAND power V_{CC} is alive, it is same with that of the Standby state.

2.2.3. Active State

Table 2.2- 3. Power consumption in active state

Mode	Operation	Item	Power Consumption Value	Units
			16 GB	
HS400	Read	I_{CC}	125	mA
		I_{CCQ}	50	mA
	Write	I_{CC}	75	mA
		I_{CCQ}	35	mA
HS200	Read	I_{CC}	88	mA
		I_{CCQ}	40	mA
	Write	I_{CC}	66	mA
		I_{CCQ}	35	mA
DDR52	Read	I_{CC}	66	mA
		I_{CCQ}	31	mA
	Write	I_{CC}	55	mA
		I_{CCQ}	31	mA

Note:

1. The measurement for max RMS current is the average RMS current consumption over a period of 100ms.
2. V_{CCQ} = 1.8V & V_{CC} = 3.3V.

2.3. Performance

Table 2.3- 1. Performance value.

Mode	Item	Performance Value	Units
		16 GB	
HS400	Sequential Write	140	MB/s
	Sequential Read	300	MB/s
HS200	Sequential Write	130	MB/s
	Sequential Read	170	MB/s
DDR52	Sequential Write	70	MB/s
	Sequential Read	80	MB/s

Note:

1. Measured on internal board, 512KB data transfer, cache on, without file system overhead.

3. Pin and Package

3.1. Signal Definition and Ball Map

Table 3.1- 1. Ball & Signal Assignment

Ball No.	Signal	Type	Description
A3	DAT0	I/O	Data I/O: These are bidirectional data signals. The DAT signals operate in push-pull mode. By default, after power-on or assertion of the RST_n signal, only DAT0 is used for data transfer. The MMC controller can configure a wider data bus for data transfer either using DAT[3:0] (4-bit mode) or DAT[7:0] (8-bit mode). eMMC includes internal pull-up resistors for data lines DAT[7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT[3:1] lines. Upon entering the 8-bit mode, the device disconnects the internal pull-ups on the DAT[7:1] lines.
A4	DAT1	I/O	
A5	DAT2	I/O	
B2	DAT3	I/O	
B3	DAT4	I/O	
B4	DAT5	I/O	
B5	DAT6	I/O	
B6	DAT7	I/O	
M5	CMD	I/O	Command: This signal is a bidirectional command channel used for command and response transfers. The CMD signal has two bus modes: open-drain mode and push-pull mode. Commands are sent from the MMC host to the device, and responses are sent from the device to the host.
M6	CLK	I	Clock: Each cycle of the clock directs a transfer on the command line and on the data line(s). The frequency can vary between the minimum and the maximum clock frequency.
K5	RST_n	I	Reset: The RST_n signal is used by the host for resetting the device, moving the device to the pre-idle state. By default, the RST_n signal is temporarily disabled in the device. The host must set EXT_CSD register byte 162, bits[1:0] to 0x1 to enable this functionality before the host can use it.
H5	DS	O	Data strobe: Generated by the device and used for data output and CRC status response output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output, each cycle of this signal directs two bits transfer (2x) on the data, one bit for the positive edge and the other bit for the negative edge. For CRC status response output, the CRC status is latched on the positive edge only, and is "Don't Care" on the negative edge.
E6	V_{CC}	P	VCC: NAND interface I/O and NAND Flash power supply
F5	V_{CC}	P	
J10	V_{CC}	P	
K9	V_{CC}	P	
C6	V_{CCQ}	P	VCCQ: eMMC controller core and eMMC I/F I/O power supply.
M4	V_{CCQ}	P	
N4	V_{CCQ}	P	
P3	V_{CCQ}	P	
P5	V_{CCQ}	P	
E7	V_{SS}	P	VSS: NAND interface I/O and NAND Flash ground connection.
G5	V_{SS}	P	
H10	V_{SS}	P	
K8	V_{SS}	P	
A6	V_{SS}	P	
J5	V_{SS}	P	

Ball No.	Signal	Type	Description
C4	V_{SSQ}	P	VSSQ: eMMC controller core and eMMC I/F ground connection.
N2	V_{SSQ}	P	
N5	V_{SSQ}	P	
P4	V_{SSQ}	P	
P6	V_{SSQ}	P	
C2	V_{DDi}	-	Internal voltage node.

Note:

(1) I/O = Bi-direction, I = Input, O = Output, P = Power/Analog

(2) VSS and VSSQ are connected internally.

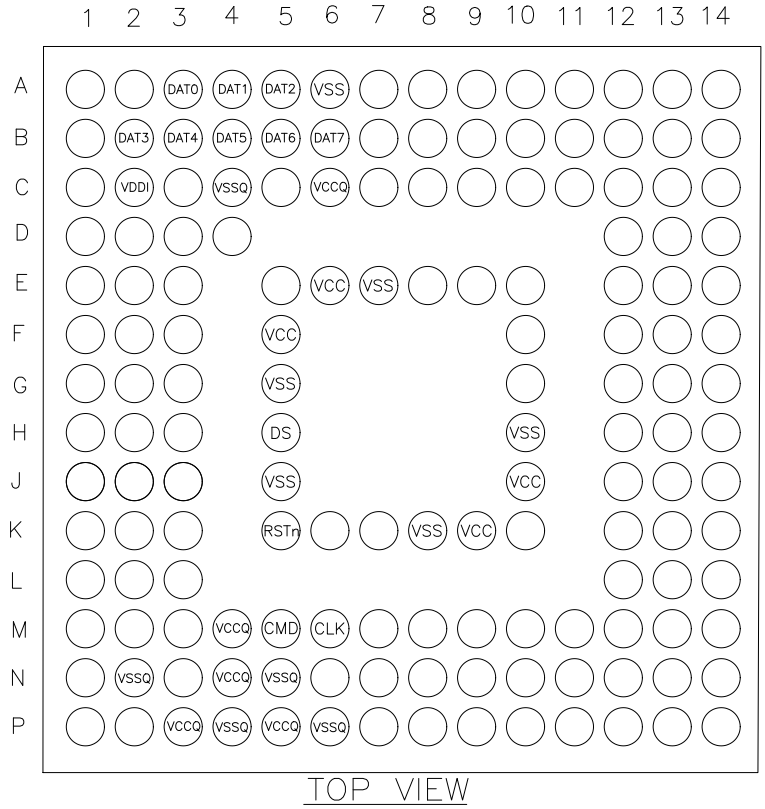

Figure 3.1- 1. Ball Mapping

3.2. Package Dimension

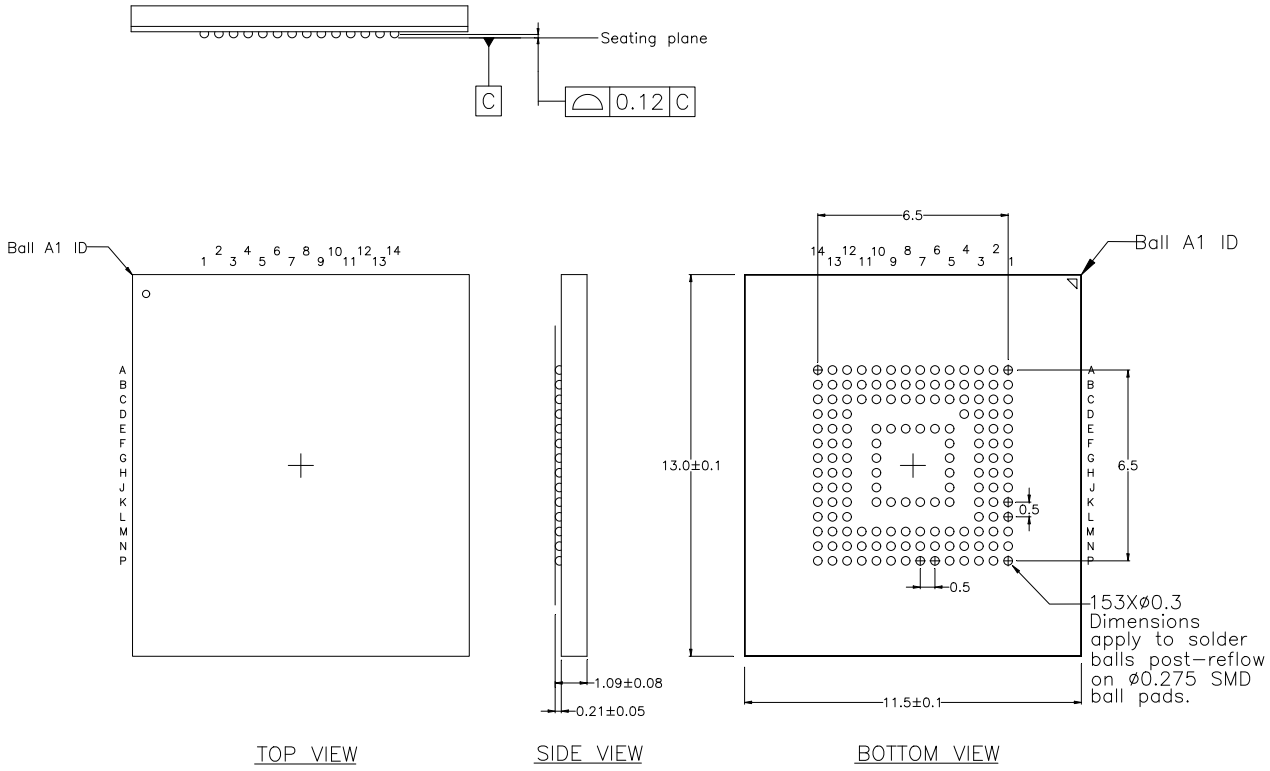

Figure 3.2- 1. Package Dimension

4. Functional Description

4.1. Architecture and Application

The eMMC device consists of a single chip eMMC controller and NAND flash memory. The controller interfaces with a host system allowing data to be written to and read from the NAND flash memory, and handles flash management, including logical to physical translation, bad block management, wear leveling and so on. The interface is only 12-bit line, can support 1-bit/4-bit/8-bit data bus flexibly. Therefore, eMMC host can integrate the eMMC easily, access it like a MMC card, and do not care about NAND flash management.

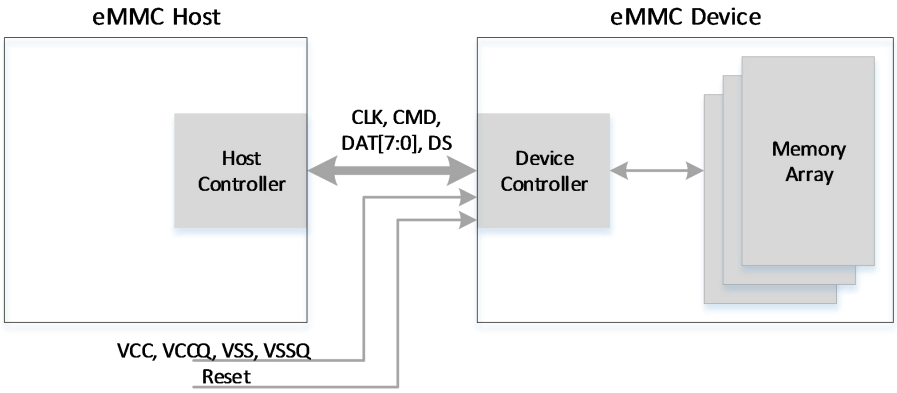

Figure 4.1- 1. eMMC System Overview

4.2. Feature List

Table 4.2- 1. Supported Feature List

Ver.	Feature	Benefit	Support
4.41	Background Operation	Better User Experience (low latency)	Y
4.41	Boot Partition and Operation		Y
4.41	Boot Partition Individual Write Protection		Y
4.41	Partitioning & Protection	Flexibility	Y
4.41	Trim		Y
4.41	Secure Erase	True Wipe	Y
4.41	Secure TRIM	True Wipe	Y
4.41	RPMB	Secure Folders	Y
4.41	Write Reliability		Y
4.41	Enhanced Reliable Write		Y
4.41	Power Off Notification	Faster Boot; Responsiveness	Y
4.41	HPI(High Priority Interrupt)	Control Long Reads/Writes	Y
4.41	HW Reset	Robust System Design	Y
4.41	Large Sector Size	Potential performance	N
4.5	HS200	Speed	Y
4.5	Extended Partition Attribute	Flexibility	Y
4.5	Packed Command	Reduce Host Overhead	Y
4.5	Discard	Improved Performance on Full Media	Y
4.5	Data Tag	Performance and/or Reliability	Y
4.5	Dynamic Capacity		Y
4.5	Context Management	Performance and/or Reliability	Y
4.5	Real Time Clock info		Y
4.5	Thermal Spec.		Y
4.5	Cache	Better Sequential & Random Writes	Y
4.51	Sanitize	True Wipe	Y
5.0	HS400	Speed	Y
5.0	Secure Removal Type		Y
5.0	Device Health Report	Vital NAND info	Y
5.0	Field Firmware Update		Y
5.0	Production State Awareness	Different operation during production	Y
5.0	Sleep Notification		Y
5.1	RPMB Throughput Improve	Faster RPMB write throughput	Y
5.1	Secure Write Protection	Secure Write Protect	Y
5.1	BKOPS Control	Host control on BKOPs	Y
5.1	Command Queuing		N
5.1	Enhanced Strobe	Sync Data out, CRC Response and CMD response between Device and Host in HS400	Y

4.3. Boot Operation

Device supports both boot mode and alternative boot mode. Device supports high speed timing and dual data rate

during boot mode.

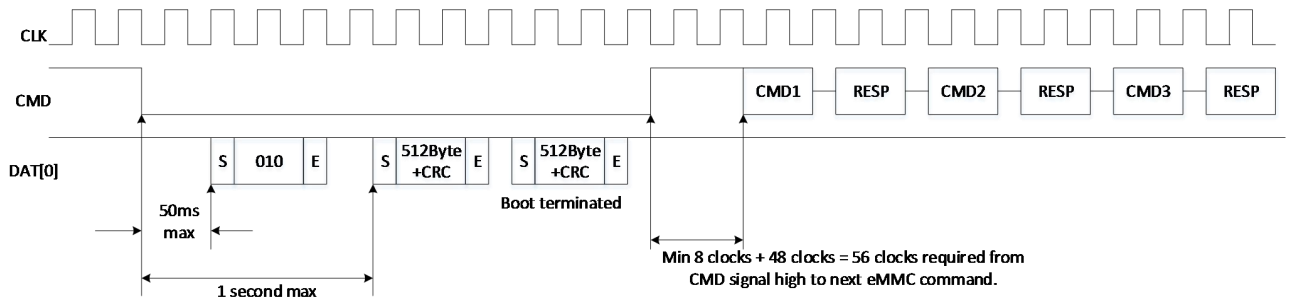

Figure 4.3- 1. eMMC Boot Mode State Diagram

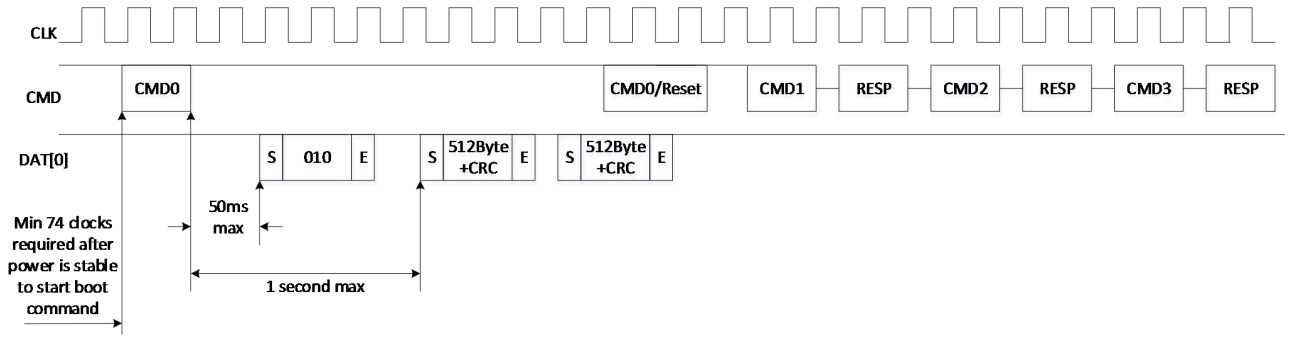

Figure 4.3- 2. eMMC Alternative Boot Mode State Diagram

Table 4.3- 1. Timing Parameter

Timing Parameter	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 1 s
(3) Initialization Time	< 1 s

4.4. H/W Reset Operation

H/W reset operation may be used to reset the device, moving the device to a Pre-idle state.
For more information, refer to JESD84-B51 standard.

4.5. Device Health Report

Device supports Device Health Report feature which can provide an estimated indication about the device life time that is reflected by the averaged wear out of memory Type A and Type B. It can be queried by standard eMMC command for getting Extended CSD structure. Please refer to below and JEDEC Standards for details.

Table 4.5- 1. Device Health Report

Field	EXT_CSD Slice	Description
DEVICE_LIFE_TIME_EST_TYP_A	268	Life time estimation of Type A(SLC) area.
DEVICE_LIFE_TIME_EST_TYP_B	269	Life time estimation of Type B(MLC/TLC) area.
PRE_EOL_INFO	267	Indication about device life time reflected by average reserved blocks

The device health feature will provide a % of the wear of the device in 10% fragments.

4.6. Field Firmware Update (FFU)

Device supports Field Firmware Updates (FFU) function to update firmware in field for those cases of debugging,

enhancing and adding new features of firmware itself. The host can download a new version of the firmware into the eMMC device by this mechanism and whole FFU process can happen without affecting any user/OS data.

The Artmem eMMC only supports Manual mode (Mode_OPERATION_CODES is not supported). For more details, see as the following chart and register table given below.

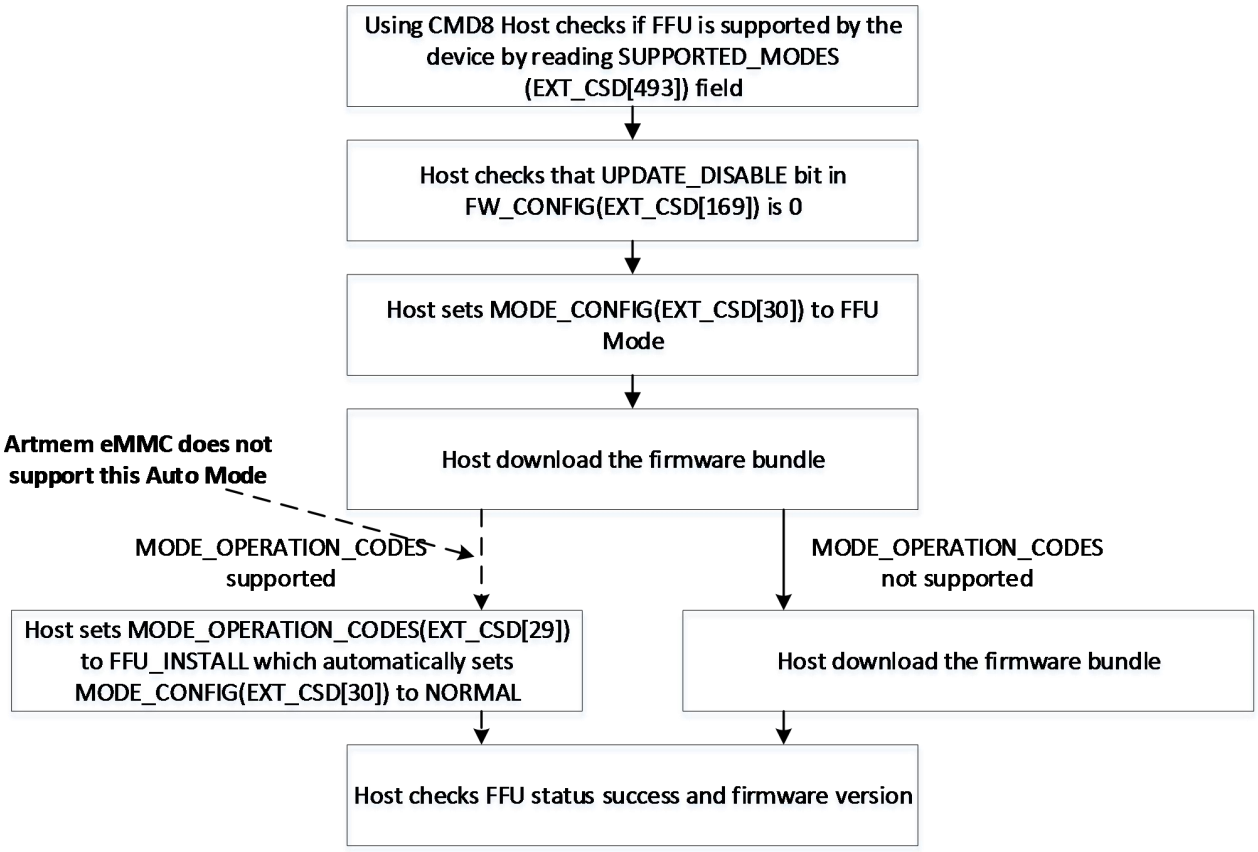

Figure 4.6- 1. FFU Flow

The Artmem eMMC Field Firmware update command flow:

Table 4.6- 1. FFU Flow

Operation	Command	Note
Initialize device to transfer mode	CMD0, ..., CMD7	
Set bus width set frequency		
Set block length to 512B	CMD16, Argu: 0x200	
Get FFU argument	CMD8	
Enter FFU mode	CMD6, Argu: 0x031E0100	
Send Firmware to device	CMD25, Argu: FFU_ARGU	
Stop data transfer	CMD12, Argu: 0x00000000	
Exit FFU mode	CMD6, Argu: 0x031E0000	
HW Reset/power cycle		
Re-initialize device to transfer mode	CMD0, CMD1,...,CMD7	
Check if FFU is succeeded	CMD8, Argu: 0x00000000	Check EXT_CSD[26], If FFU_SUCCESS is 0, FFU is succeeded, otherwise FFU is failed.

4.6.1. EXT_CSD Register for FFU

1. SUPPORTED_MODE[493] (Read Only)

Table 4.6- 2. EXT_CSD[493]

Bit	Field	Supportability
Bit[7:2]	Reserved	-
Bit[1]	VSM	Not support
Bit[0]	FFU	Supported

BIT[0] :
- 0: FFU is not supported by the device.
- 1: FFU is supported by the device.

BIT[1] :
- 0: Vendor specific mode(VSM) is not supported by the device.
- 1: Vendor specific mode is supported by the device

2. FFU_FEATURE[492] (Read Only)

Table 4.6- 3. EXT_CSD[492]

Bit	Field	Supportability
Bit[7:1]	Reserved	-
Bit[0]	SUPPORTED_MODE_OPERATION_CODES	Not support

BIT[0] :
- 0: Device does not support MODE_OPERATION_CODES field.
- 1: Device supports MODE_OPERATION_CODES field.

3. FFU_ARG[490-487] (Read Only)

Using this field the device reports to the host which value the host should set as an argument for the read and write commands in FFU mode.

4. FFU_CONFIG[169] (R/W)

Table 4.6- 4. EXT_CSD[169]

Bit	Field	Supportability
Bit[7:1]	Reserved	-
Bit[0]	Update Disable	Firmware updates enabled (0x0)

BIT[0] :
- 0: Enable update Firmware.
- 1: Disable update Firmware permanently.

5. FFU_STATUS[26] (R/W/E_P)

Using this field the device reports the status of the FFU process.

Table 4.6- 5. EXT_CSD[26]

Value	Description
0x00	Success
0x01-0x0F	Reserved
0x10	General Error
0x11	Firmware Install Error
0x12	Error in Downloading Firmware
Others	Reserved

6. OPERATION_CODES_TIMEOUT[491](Read Only)

Maximum timeout for the SWITCH command when setting a value to the MODE_OPERATION_CODES field. The register is set to '0', because the device does not support MODE_OPERATION_CODES.

Table 4.6- 6. EXT_CSD[491]

Value	Description
0x00	0x0 (Not Defined)
Others	Reserved

7. MODE_OPERATION_CODES[29] (W/E_P)

The host sets the operation to be performed at the selected modes, in case MODE_CONFIGS is set to FFU_MODE, MODE_OPERATION_CODES could have the following values.

The Artmem device does not support MODE_OPERATION_CODES.

Table 4.6- 7. EXT_CSD[29]

Value	Description
0x00	Reserved
0x01	FFU_INSTALL
0x02	FFU_ABORT
Others	Reserved

8. MODE_CONFIG [30] (R/W/E_P)

Using this field the host can change the mode of the device

Table 4.6- 8. EXT_CSD[30]

Value	Description
0x00	Normal Mode (To keep the compatibility)
0x01	FFU Mode
0x02	Vendor Specific Mode
Others	Reserved

4.7. Auto Power Saving Mode

If host does not issue any command during certain duration, the device will enters power saving mode to reduce power consumption. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device.

When the host is ready to access a device at any time, any command issued to device will cause it to exit sleep and respond immediately.

4.8. Sleep (CMD5)

The Device support using sleep/awake command (CMD5) to switch between a sleep and a standby state. In the sleep state the power consumption of the device is minimized and the device reacts only to the commands reset command (CMD0) and awake command (CMD5).

The VCC power supply support to be switched off in sleep state to minimize power consumption.

For more information, refer to JESD84-B51 standard.

5. Register Value

Within the device interface, six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. All of them can be accessed only corresponding commands. For detail information, please refer JESD84-B51 standard. The OCR, CID and CSD registers has information of device and content, while the RCA and DSR registers are for configuring parameters of device. For the EXT_CSD register, it contains both device specific information and actual configuration parameters.

Following sections are for describing all register value of eMMC device at its default. And these values here may be updated in later version without notice.

5.1. OCR Register

The 32-bit operation conditions register (OCR) contains: VCC voltage profile of the device, access mode indication, status information bit. The status bit is set when the device finished its power up procedure.

Table 5.1- 1. OCR Register

OCR bit	V_{CCQ} Voltage Window	Register Value
[6:0]	Reserved	000 0000b
[7]	1.70 ~ 1.95	1b
[14:8]	2.0 ~ 2.6	000 0000b
[23:15]	2.7 ~ 3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b (sector mode)
[31]	eMMC power up status bit (busy). This bit is set to LOW during the busy of power up routine.	

5.2. CID Register

The card identification (CID) register is 128 bits wide. It contains the device identification information used during the card identification phase as required by eMMC protocol. Each device shall have a unique identification number.

Table 5.2- 1**. CID Register**

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0xEC
Reserved	6	[119:114]	---	0x0
Card/BGA	CBX	2	[113:112]	0x01
OEM/Application ID	OID	8	[111:104]	0x00
Product name	PNM	48	[103:56]	16GB: 0x41 54 32 30 31 36(ASCII: AT2016)
Product revision	PRV	8	[55:48]	0x10
Product serial number	PSN	32	[47:16]	-
Manufacturing date	MDT	8	[15:8]	-
CRC7 checksum	CRC	7	[7:1]	-
not used, always '1'	-	1	[0:0]	-

5.3. CSD Register

The device Specific Data (CSD) register provides information on how to access the device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E) can be changed by CMD27.
For more information, refer to JESD84-B51 standard.

Table 5.3- 1**. CSD Register**

Name	Field	Width	Type	CSD-slice	Value

Name	Field	Width	Type	CSD-slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	0x00
Data read access-time 1	TAAC	8	R	[119:112]	0x2F
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Device command classes	CCC	12	R	[95:84]	0x8F5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved	-	2	R	[75:74]	0x00
Device size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x07
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x07
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x07
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x07
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x0F
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	R	[20:17]	0x00
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x00
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	
Not used, always'1'	-	1	—	[0:0]	

Note:
1. Register type explanations:

(1) R = Read-only.
(2) R/W = One-time programmable and readable.
(3) R/W/E = Multiple writable with value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.
2. Reserved bits should be read as 0.

5.4. Extended CSD Register

Table 5.4- 1. Extended CSD Register

Name	Field	Size	Type	CSD-slice	Value	Note
Reserved	-	6	TBD	[511:506]	0x00	
Extended Security Command Error	EXT_SECURITY_ERR	1	R	[505]	0x00	
Supported Command Set	S_CMD_SET	1	R	[504]	0x01	
HPI features	HPI_FEATURES	1	R	[503]	0x01	
Background operation support	BKOPS_SUPPORT	1	R	[502]	0x01	
Max packed read commands	MAX_PACKED_READS	1	R	[501]	0x3F	
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	0x3F	
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	0x01	
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0x00	
Tag Resource Size	TAG_RES_SIZE	1	R	[497]	0x00	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	0x05	
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	0x07	
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	0x03	
Supported modes	SUPPORTED_MODES	1	R	[493]	0x01	
FFU features	FFU_FEATURES	1	R	[492]	0x00	
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	0x00	
FFU Argument	FFU_ARG	4	R	[490:487]	0xFFFFFF5F	
Barrier support	BARRIER_SUPPORT	1	R	[486]	0x01	
Reserved		177	TBD	[485:309]	0x00	
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	0x00	
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	0x0F	
Reserved		1		[306]	0x00	
Number of FW sectors correctly programed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0x00	

Name	Field	Size	Type	CSD-slice	Value	Note
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	0x00	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0x01	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0x01	
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0x01	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	0x40	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	0x40	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	0x07	
Device version	DEVICE_VERSION	2	R	[263:262]	0x203	
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	-	FW Version
Power class for 200MHz, DDR at VCC=3.6	PWR_CL_DDR_200_360	1	R	[253]	0xDD	
Cache size	CACHE_SIZE	4	R	[252:249]	0x00000400	
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	0x64	
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	0x8C	
Background operation status	BKOPS_STATUS	1	R	[246]	0x00	
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00	
1st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x0A	
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0x01	
Power class for 52MHz, DDR at VCC=3.6V	PWR_CL_DDR_52_360	1	R	[239]	0xAA	
Power class for 52MHz, DDR at VCC=1.95V	PWR_CL_DDR_52_195	1	R	[238]	0xDD	
Power class for 200MHz at VCCQ=1.95V, VCC=3.6V	PWR_CL_200_195	1	R	[237]	0xDD	
Power class for 200MHz at VCCQ=1.3V, VCC=3.6V	PWR_CL_200_130	1	R	[236]	0xDD	

Name	Field	Size	Type	CSD-slice	Value	Note
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00	
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00	
Reserved		1	TBD	[233]	0x00	
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x16	
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x55	
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x02	
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x02	
Boot information	BOOT_INF	1	R	[228]	0x07	
Reserved		1	TBD	[227]	0x00	
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	0x20	
Access size	ACC_SIZE	1	R	[225]	0x07	
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01	
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x16	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01	
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x10	
Sleep current (Vcc)	S_C_VCC	1	R	[220]	0x08	
Sleep current (VccQ)	S_C_VCCQ	1	R	[219]	0x08	
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	0x0A	
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x17	
Sleep Notification Timeout	SLEEP_NOTIFICATIN_TIME	1	R	[216]	0x11	
Sector Count	SEC_COUNT	4	R	[215:212]	0x01D20000	
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0x01	
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0x0A	

Name	Field	Size	Type	CSD-slice	Value	Note
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0x0A	
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x0A	
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x0A	
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0x0A	
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0x0A	
Reserved		1	TBD	[204]	0x00	
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	R	[203]	0x22	
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	R	[202]	0xAA	
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	R	[201]	0x22	
Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	R	[200]	0xAA	
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x32	
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x0A	
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0x1F	
Device type	DEVICE TYPE	1	R	[196]	0x57	
Reserved		1	TBD	[195]	0x00	
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	0x02	
Reserved		1	TBD	[193]	0x00	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	0x08	
Command set	CMD_SET	1	R/W/E_P	[191]	0x00	
Reserved		1	TBD	[190]	0x00	
Command set revision	CMD_SER_REV	1	R	[189]	0x00	
Reserved		1	TBD	[188]	0x00	
Power class	POWER_CLASS	1	R/W/E_P	[187]	0x00	

Name	Field	Size	Type	CSD-slice	Value	Note
Reserved		1	TBD	[186]	0x00	
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	0x00	
Strobe Support	STROBE_SUPPORT	1	R	[184]	0x01	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0x00	
Reserved		1	TBD	[182]	0x00	
Erased memory content	ERASED_MENM_CONT	1	R	[181]	0x00	
Reserved		1	TBD	[180]	0x00	
Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	[179]	0x00	
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0x00	
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0x00	
Reserved		1	TBD	[176]	0x00	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00	
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0x00	
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00	
Reserved		1	TBD	[172]	0x00	
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0x00	
Reserved		1	TBD	[170]	0x00	
FW configuration	FW_CONFIG	1	R/W	[169]	0x00	
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x20	
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F	
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x15	
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0x00	
Manually start backgroud operations	BKOPS_START	1	W/E_P	[164]	0x00	

Name	Field	Size	Type	CSD-slice	Value	Note
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0x00	
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00	
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00	
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	0x07	
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x000026D	
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00	
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0x00	
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00	
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00	
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00	
Reserved		1	TBD	[135]	0x00	
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0x00	
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0x00	
Package Case Terperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0x00	
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0x00	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0x00	
Reserved		2	TBD	[129:128]	0x00	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	vendor or specific	[127:64]	-	
Native sector size	USE_NATIVE_SECTOR	1	R	[63]	0x00	
Sector size emulation	NATIVE_SECTOR_SIZE	1	R/W	[62]	0x00	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0x00	
1st initiallization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0x00	
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0x00	
number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0x00	

Name	Field	Size	Type	CSD-slice	Value	Note
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0x00	
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0x00	
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0x00	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0x00	
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0x00	
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0x00	
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0x00	
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0x00	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0x00	
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0x00	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0x00	
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0x00	
Reserved		2	TBD	[28:27]	0x00	
FFU status	FFU_STATUS	1	R	[26]	0x00	
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0x00	
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	0x009B4000	
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	0x01	
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	0x39	
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0x00	
Reserved		15	TBD	[14:0]	0x00	

Note:
1. Register type explanations:
(1) R = Read-only.
(2) R/W = One-time programmable and readable.
(3) R/W/E = Multiple writable with the value kept after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.
(4) R/W/C_P = Writable after the value is cleared by a power cycle and assertion of the RST_n signal (the value not

cleared by CMD0 reset) and readable.
(5) R/W/E_P = Multiple writable with the value reset after a power cycle, assertion of the RST_n signal, and any CMD0 reset, and readable.
(6) W/E_P = Multiple writable with the value reset after power cycle, assertion of the RST_n signal, and any CMD0 reset, and not readable.
2. Reserved bits should be read as 0.

5.5. RCA Register

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

6. Electrical Characteristics

6.1. Supply Voltage

Table 6.1- 1. Supply Voltage

Item	Min	Max	Unit
VCCQ	1.7	1.95	V
	2.7	3.6	V
VCC	2.7	3.6	V
VSS	-0.5	0.5	V

6.2. Bus Signal Line Load

The total capacitance C_L of each line of the eMMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the eMMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

Table 6.2- 1. Bus Signal Line Load

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	Kohm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	Kohm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	Kohm	to prevent unconnected lines floating
Single Device capacitance	C_{DEVICE}			30	pF	
Maximum signal line inductance				16	nH	fPP <= 52 MHz

Table 6.2- 2. Capacitance and Resistance for HS400 mode

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Bus signal line capacitance	C_L			13	pF	Single Device
Single Device capacitance	C_{DEVICE}			6	pF	

Pull-down resistance for Data Strobe	$R_{Data\ Strobe}$	10		100	Kohm	

6.3. Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

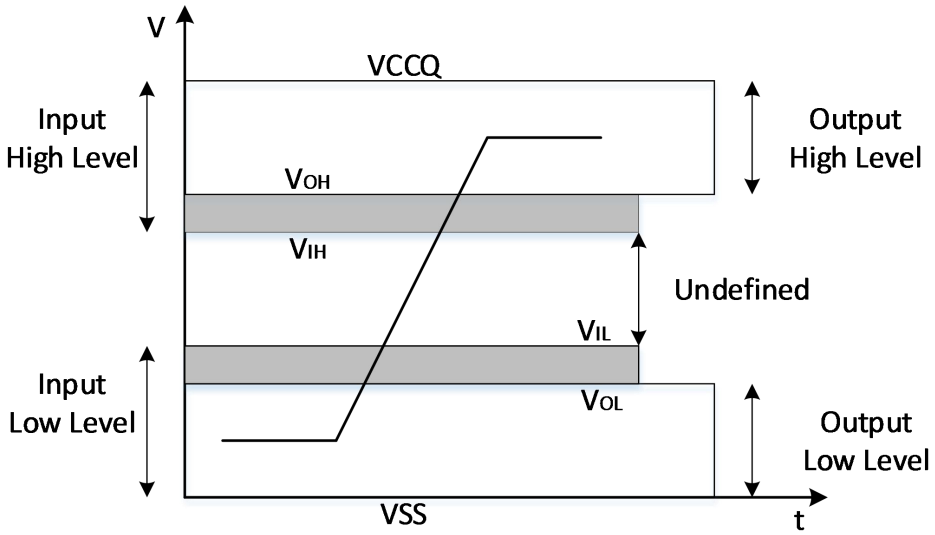

Figure 6.3- 1. Bus Signal Levels

Table 6.3- 1**. Bus Signal Levels**

Parameter	Symbol	Min	Max	Unit	Remark
Open-drain mode					
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.2	-	V	(1)
Output LOW voltage	V_{OL}	-	0.3	V	
Push-pull mode (VCCQ: 2.7V - 3.6V)					
Output HIGH voltage	V_{OH}	0.75 * V_{CCQ}	-	V	I_{OH} = -100uA @ V_{CCQ} min
Output LOW voltage	V_{OL}	-	0.125 * V_{CCQ}	V	I_{OL} = 100uA @ V_{CCQ} min
Input HIGH voltage	V_{IH}	0.625 * V_{CCQ}	V_{CCQ} + 0.3	V	-
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25 * V_{CCQ}	V	-
Push-pull mode (VCCQ: 1.70V - 1.95V)					
Output HIGH voltage	V_{OH}	V_{CCQ} - 0.45	-	V	I_{OH} = -2mA
Output LOW voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65 * V_{CCQ}	V_{CCQ} + 0.3	V	(2)
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35 * V_{CCQ}	V	(3)

NOTE:
(1) Because V_{OH} depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet V_{OH} Min value.
(2) 0.7 x V_{CCQ} for MMC4.3 and older revisions.
(3) 0.3 x V_{CCQ} for MMC4.3 and older revisions.

6.4. Bus Timing Specification

The Artmem eMMC follows JEDEC standard, for timing specification of all bus mode, including High Speed SDR, High Speed DDR, HS200, HS400, please refer to JESD84-B51 standard.

7. Design Guide

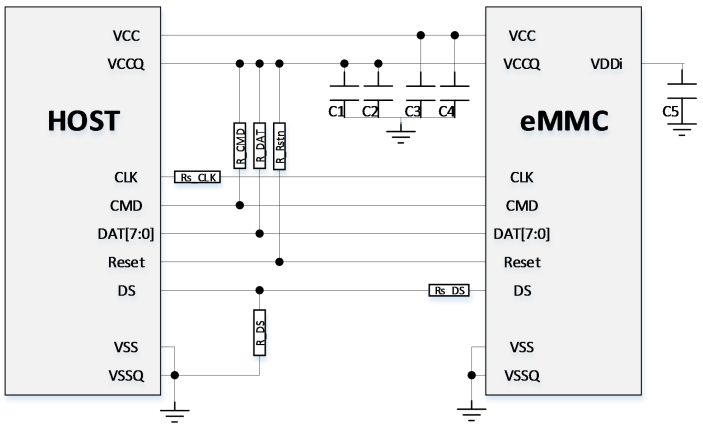

Figure 6.4- 1 eMMC Connect Guide

Table 6.4- 1. Component recommendation

Description	Symbol	Min.	Max.	Typ.	Unit	Note
Pull-up resistance for CMD	R_CMD	4.7	100	10	Kohm	Pull-up resistance should be put on CMD line to prevent bus floating.
Pull-up resistance for DAT0~7	R_DAT	10	100	50	Kohm	Pull-up resistance should be put on DAT line to prevent bus floating.
Data strobe(DS)	R_DS	10	100	10	Kohm	Pull-down resistance should be put on DS line to prevent bus floating.
Serial resistance on DS	Rs_DS	0	30	0	ohm	To reduce overshooting/undershooting Note: If the host uses HS400, we recommend to remove this resister for better DS signal.
Pull-up resistance for Rstn	R_Rstn	10	100	50	Kohm	It is not necessary to put pull-up resistance on Rstn line if host does not use H/W reset. (Extended CSD register [162] = 0b)
Serial resistance on CLK	Rs_CLK	0	30	0	ohm	To reduce overshooting/undershooting Note: If the host uses HS200/HS400, we recommend to remove this resister for better CLK signal.
VCCQ capacitor value	C1	1	10	2.2	uF	Coupling capacitor should be connected with VCCQ and VSSQ as closely as possible.
	C2	0.1	0.22	0.1	uF	
VCC capacitor value	C3	1	10	2.2	uF	Coupling capacitor should be connected with VCC and VSS as closely as possible.
	C4	0.1	0.22	0.1	uF	
VDDi capacitor value	C5	0	0.1	0	uF	Coupling capacitor should be connected with VDDi and VSSQ as closely as possible. No capacitor is recommended.

Description	Symbol	Min.	Max.	Typ.	Unit	Note
CLK/CMD/DS/DAT[7:0] impedance		45	55	50	ohm	For impedance match.