

Low Power HDMI Transmitter

EP952(B)

Data Sheet

V0.5

Revised: Apr. 02, 2012

Original Release Date: Sep. 27, 2010

Explore

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Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Sep/27/2010	Ether Lai	Initial Version
0.1	Dec/01/2010	Ether Lai	Add the Pin Diagram of BGA-64 package; Add the detailed package outline dimension; Update BGA-64 package outline dimension;
0.2	Apr/11/2011	Ether Lai	Add the Ordering Information for different type of chip configuration; Revise Package Footprint Diagram; Fix typo in Register Description;
0.3	Mar/03/2011	Ether Lai	Add the Thermal Resistance;
	Sep/14/2011	Kyle Kuo	Add the Power Consumption Revised EXT_SWING Resistor Value to 820 Ohm
0.4	Nov/24/2011	Kyle Kuo	Remove Device Part of K Serial
0.5	Apr/02/2012	Ether Lai	Separate the User Guide to Data Sheet & User Guide; Fix the Typos;

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Section 1 Introduction

1.1 Overview

EP952(B) is a Low Power HDMI (High Definition Multimedia Interface) transmitter. The chip is compliant with HDMI Rev 1.4 and HDCP Rev 1.4 specifications. The chip converts input video data in RGB or YUV format and audio data in IIS or SPDIF format into HDMI differential signals. The chip supports 8-bit video upto 1080p in HDMI mode. The chip also supports 3D video. The chip supports highly flexible digital video input in a muxed 12-bits mode or non-muxed 24-bit mode input. In both modes, the chip supports single or dual edge clocking.

1.2 Features

- HDMI Specification 1.4 Compliant
- Integrated HDCP encryption engine which is compliant with HDCP Rev 1.4 specification for transmitting protected content
- Integrated on-chip HDCP Keys (Optional)
- Wide TMDS Clock Frequency Range: 25MHz - 165MHz in HDMI mode
- Support 8-bit video upto 1080p in HDMI mode
- Support 3D video
- Support IIS and SPDIF (LPCM or compressed) audio types
- Support auto-send for DVI, ADO, ACR (Audio Clock Regeneration) and General Control packets.
- Support 1 Generic Data Packet buffer
- Flexible digital video input: muxed 12-bit and non-muxed 24-bit mode in RGB or YUV, embedded sync or separate sync
- Support 1 port of SPDIF audio input (without the need for system clock) and 2 channels of IIS audio inputs
- Supports audio down sampling at 1/2, 1/3 or 1/4 sampling rate for both SPDIF and IIS
- Supports CCIR YUV422 format input
- On-chip YUV422 to YUV444 conversion and YUV444 to YUV422 conversion
- On-chip YUV to RGB and RGB to YUB conversion in ITU-R BT.601 and 709 color space
- Register Programmable Single/Dual Edge Clocking Mode
- IIC Slave Programming Interface
- Programmable DE generation
- Supports x2, x4 and x8 Pixel Repetition
- Supports input De-Skewing

- Supports Receiver Hot Plug Detection
- Downward compatible with DVI 1.0
- Supports Power Down Mode
- 3.3V and 1.8V power required

1.3 Ordering Information

Two parts with different Package Type and HDCP Key Configuration are provided:

Table 1-1 EP952 Ordering Information

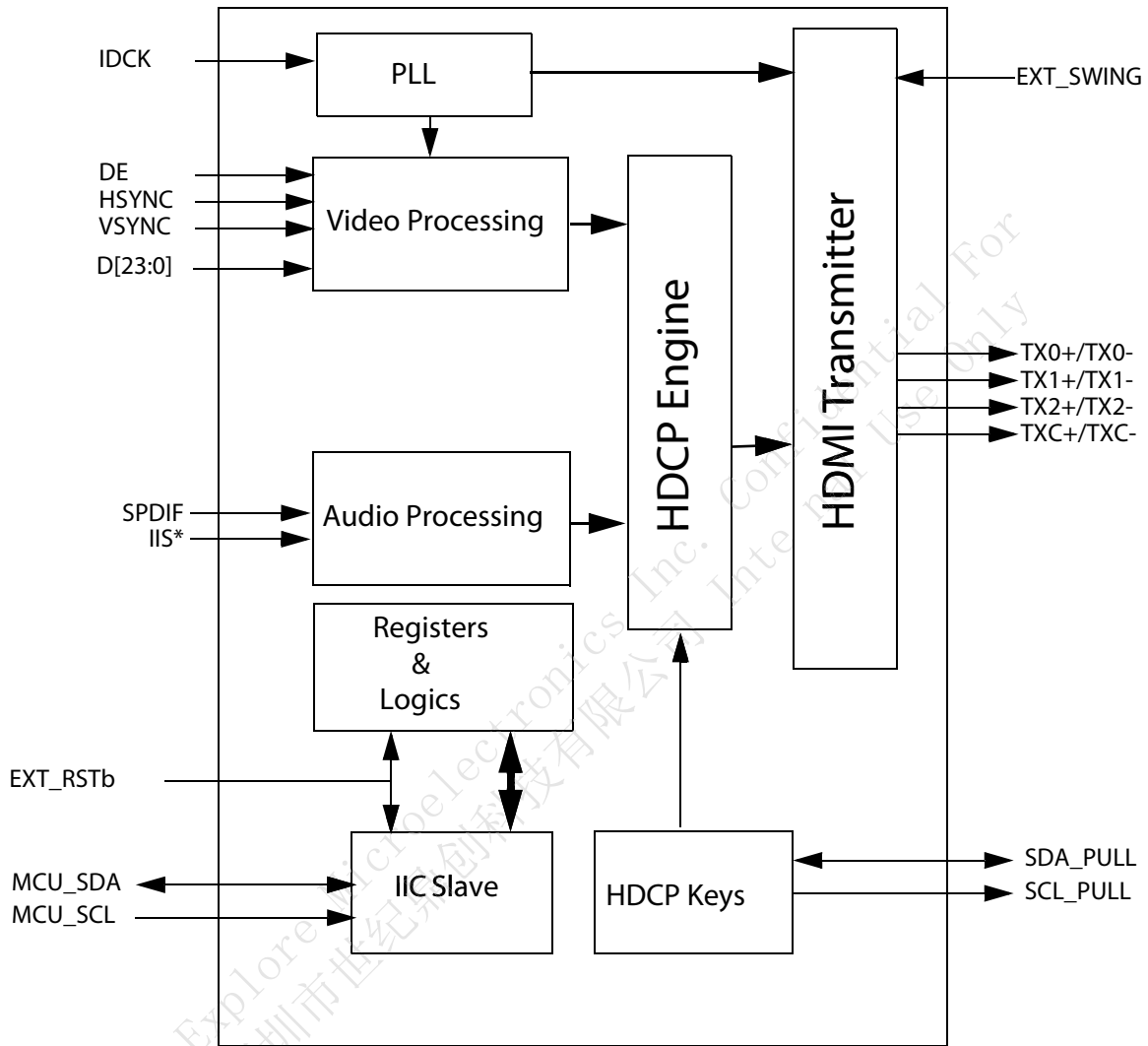
Device Part #	Package Type	Pins	HDCP Keys
EP952	LQFP-64 (7mm x 7mm)	64	Write from External MCU
EP952B	BGA-64 (5mm x 5mm)	64	Write from External MCU

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Section 2 Overview

2.1 Block Diagram

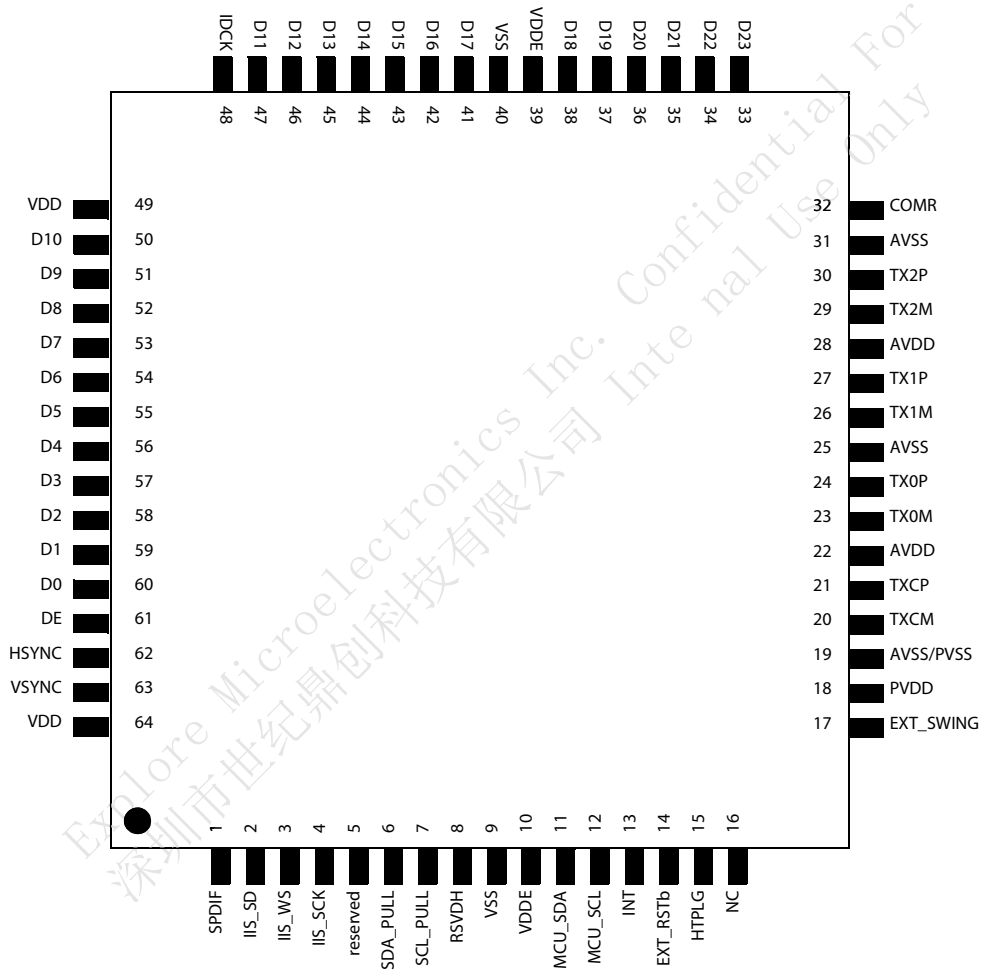
Figure 2-1 Block Diagram



2.2 Pin Diagram

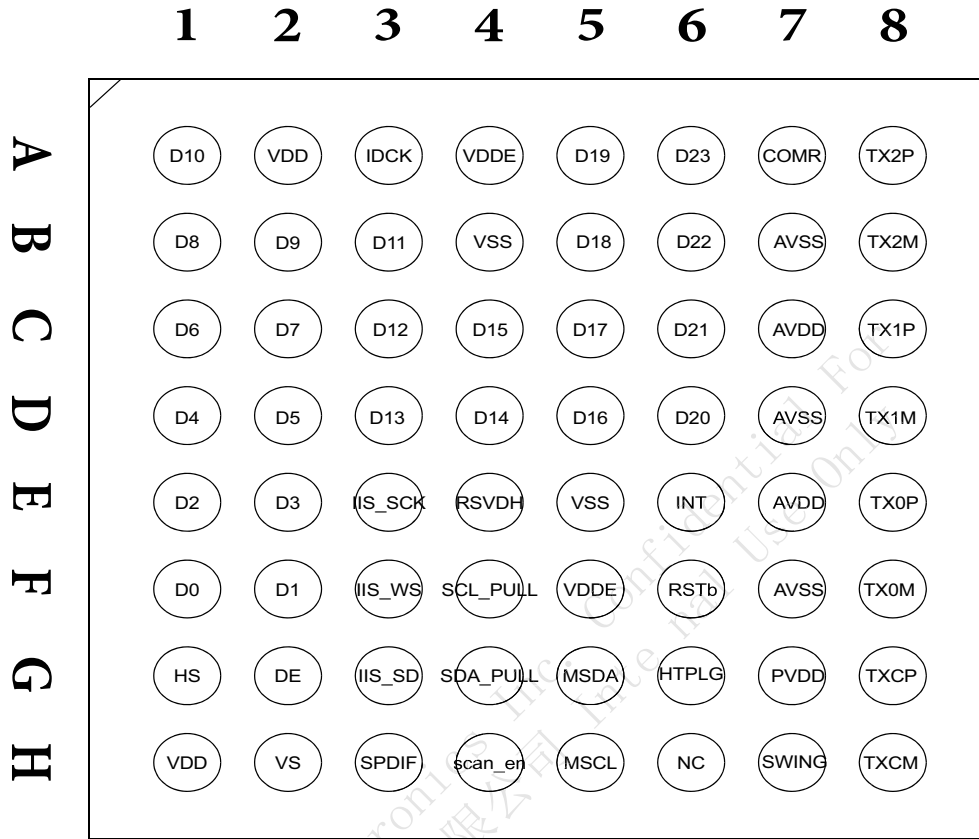
2.2.1 LQFP-64

Figure 2-2 Pin Diagram (LQFP-64)

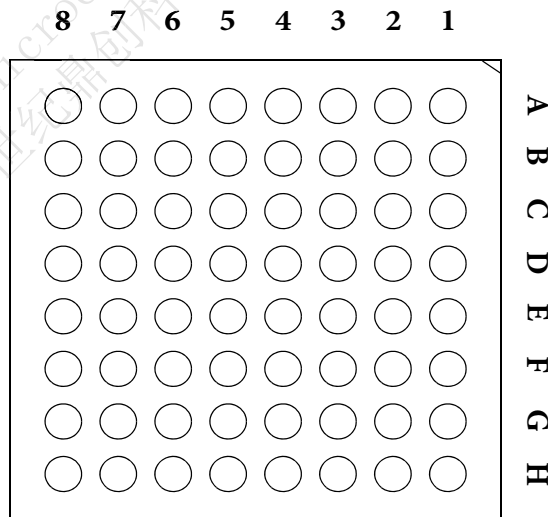


2.2.2 BGA-64

Figure 2-3 Pin Diagram (BGA64)



TOP View



Bottom View

2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Input Control/Data/CLK Pins

NAME	IN / OUT	DESCRIPTION
D23 - D12	IN	Top half of 24-bit pixel bus When BSEL = HIGH, this bus inputs the top half of the 24-bit pixel bus When BSEL = LOW, these bits are not used to input pixel data. In this mode, the state of D[23:16] is input to the IIC register CFG. This allow 8-bits of user configuration data to be read by the graphics controller through the IIC interface. D[15:12] are not used and should be tied to GND.
D11 - D0	IN	Bottom half of 24-bit pixel bus / 12-bit pixel bus input When BSEL = HIGH, this bus inputs the bottom half of the 24-bit pixel bus When BSEL = LOW, this bus inputs 1/2 a pixel (12-bits) at every latch edge (both falling and/or rising) of the clock.
IDCK	IN	Input Data Clock
DE	IN	Data Enable Input. This signal is high when input pixel data is valid to the transmitter and low otherwise. It is critical that this signal have the same setup/hold timing as the data bus.
HSYNC	IN	Horizontal Sync Input.
VSYNC	IN	Vertical Sync Input.

Table 2-2 Audio Input Pins

NAME	IN / OUT	DESCRIPTION
SPDIF	IN	SPDIF audio port input
IIS_SCK	IN	IIS SCK input for IIS audio port
IIS_WS	IN	IIS WS input for IIS audio port
IIS_SD	IN	IIS SD input for IIS audio port

Table 2-3 IIC Pins

NAME	IN / OUT	DESCRIPTION
MCU_SCL	IN	SCL signal for slave IIC port
MCU_SDA	IO	SDA signal for slave IIC port
SCL_PULL	OUT	Pull-up this pin to 3V3 through 4.7KΩ resistor.
SDA_PULL	IO	Pull-up this pin to 3V3 through 4.7KΩ resistor.
RSVDH	IN	Connect this pin to 3.3V for normal operation.

Table 2-4 Misc. Pins

NAME	IN / OUT	DESCRIPTION
EXT_RSTb	IN	External Reset (Active LOW). A HIGH level indicates normal operation and a LOW level causes all the logic on the chip to be reset.

Table 2-4 Misc. Pins

NAME	IN / OUT	DESCRIPTION
INT	OUT	Interrupt. This pin is an open drain or push-pull output. The output polarity and interrupt source are programmable through the IIC interface.
reserved	IN	Must be tied LOW for normal operation.
NC	IO	Must be left Open for normal operation.

Table 2-5 Differential Signal Data Pins

NAME	IN / OUT	DESCRIPTION
TX0- TX0+ TX1- TX1+ TX2- TX2+	Analog	Differential Data Output Pairs for HDMI.
TXC+ TXC-	Analog	Differential Clock Output Pairs for HDMI
EXT_SWING	Analog	Voltage Swing Adjust. A resistor should tie this pin to AVCC. This resistance determines the amplitude of the voltage swing. 820ohm is recommended.
COMR	Analog	For connecting a 0.1uF cap to AVSS
HTPLG	IN	HDMI Hot Plug Input. This pin is used to monitor the "HOT PLUG" signal in HDMI mode. Note: This input is 5V tolerant.

Table 2-6 Power and Ground Pins

NAME	IN / OUT	DESCRIPTION
VDDE	PWR	Digital IO Power, 3.3 V
VDD	PWR	Digital Power, 1.8 V
VSS	GND	Digital/IO Ground
AVDD	PWR	Analog Power for HDMI transmitter, 1.8V
AVSS	GND	Analog Ground for HDMI transmitter
PVDD	PWR	Analog Power for PLL, 1.8V
PVSS	GND	Analog Ground for PLL

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC33}	3.3V Supply Voltage	-0.3		4.0	V
V _{CC18}	1.8V Supply Voltage	-0.3		2.5	V
V _I	Input Voltage	-0.3		V _{CC33} + 0.3	V
V _O	Output Voltage	-0.3		V _{CC33} + 0.3	V
T _J	Junction Temperature			125	°C
T _{STG}	Storage Temperature	-40		125	°C
θ _{JA_LQFP}	Thermal Resistance (Junction to Ambient; LQFP)		58		°C/W
θ _{JA_BGA}	Thermal Resistance (Junction to Ambient; BGA)		54		°C/W

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC33}	3.3V Supply Voltage	3.14	3.3	3.6	V
V _{CC18}	1.8V Supply Voltage	1.71	1.8	1.98	V
V _{CCN}	Supply Voltage Noise ¹	-0.3		100	mV _{p-p}
T _A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	High-level Input Voltage		1.6			V
V _{IL}	Low-level Input Voltage				0.6	V
V _{OH}	High-level Output Voltage		2.4			V
V _{OL}	Low-level Output Voltage				0.4	V
I _{OL}	Output Leakage Current	High Impedance	-10		10	uA

DC Analogue Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Voltage Single ended peak to peak amplitude	$R_{LOAD} = 50 \text{ ohm}$ $R_{EXT_SWING} = 820 \text{ ohm}$	510	550	590	mV
V_{DOH}	Differential High-level Output Voltage			AVCC		mV
I_{DOS}	Differential Output Short Circuit Current	$V_{OUT} = 0V$			5	uA
I_{PD}	Power-Down Current ²	25°C Ambient, VDDE=3.3V VDD=AVDD=PVDD=1.8V		40		uA
I_{CCD}	1.8 V Operating Current $R_{EXT_SWING} = 820 \text{ ohm}$	DCLK = 25.2 Mhz Normal Pattern		65		mA
		DCLK = 74.25 Mhz Normal Pattern		90		mA
		DCLK = 148.5 Mhz Normal Pattern		135		mA
	3.3 V Operating Current $R_{EXT_SWING} = 820 \text{ ohm}$	DCLK = 25.2 Mhz Normal Pattern		1.2		mA
		DCLK = 74.25 Mhz Normal Pattern		1.6		mA
		DCLK = 148.5 Mhz Normal Pattern		2.3		mA

AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{CIP}	IDCK Period, 1-pixel/clock		6.06		40	ns
F_{CIP}	IDCK Frequency, 1-pixel/clock		25		165	MHz
T_{CIH}	IDCK High Time at 165MHz		2.0			ns
T_{CIL}	IDCK Low Time at 165MHz		2.0			ns
T_{JIT}	Worst Case IDCK Clock Jitter ^{2,3}				2	ns
T_{SIDF}	Data, DE VSYNC, HSYNC Setup Time to IDCK falling edge	Single Edge (DSEL=0, DKEN=0, EDGE=0)	1.0			ns
T_{HIDF}	Data, DE VSYNC, HSYNC Hold Time to IDCK falling edge	Single Edge (DSEL=0, DKEN=0, EDGE=0)	0.9			ns
T_{SIDR}	Data, DE VSYNC, HSYNC Setup Time to IDCK rising edge ¹	Single Edge (DSEL=0, DKEN=0, EDGE=1)	1.0			ns
T_{HIDR}	Data, DE VSYNC, HSYNC Hold Time to IDCK rising edge ¹	Single Edge (DSEL=0, DKEN=0, EDGE=1)	0.9			ns

T_{SID}	Data, DE VSYNC, HSYNC Setup Time to IDCK falling/rising edge ¹	Dual Edge (DSEL=1, DKEN=0, EDGE=0)	0.6			ns
T_{HID}	Data, DE VSYNC, HSYNC Hold Time to IDCK falling/rising edge ¹	Dual Edge (DSEL=1, DKEN=0, EDGE=0)	1.3			ns
T_{DDF}	VSYNC, HSYNC delay from DE falling edge ¹		$1T_{CIP}$			ns
T_{DDR}	VSYNC, HSYNC delay from DE rising edge ¹		$1T_{CIP}$			ns
T_{HDE}	DE High Time ¹	Vertical Blanking Only			$8191T_{CIP}$	ns
T_{LDE}	DE Low Time ^{1,4}	Vertical Blanking Only	$128T_{CIP}$			ns
T_{STEP}	De-skew step size increment	DKEN = 1		260		ps
S_{LHT}	Differential Swing Low-to-High Transition Time	$C_{LOAD} = 5pF,$ $R_{LOAD} = 50\text{ ohm},$ $R_{EXT_SWING} = 820\text{ ohm}$	170	200	230	ps
S_{HLT}	Differential Swing High-to-Low Transition Time	$C_{LOAD} = 5pF,$ $R_{LOAD} = 50\text{ ohm},$ $R_{EXT_SWING} = 820\text{ ohm}$	170	200	230	ps

1 Guaranteed by design.

2 Jitter can be estimated by 1) triggering a digital scope at the rising of input clock and 2) measuring the peak to peak time spread of the rising edge of the input clock at both 0.5us and 1.0us after the trigger.

3 Actual jitter tolerance may be higher depending on the frequency of the jitter.

4 DE low time as defined as per DVI 1.0 specification, Section 3.4 Link Timing Requirement.

Figure 2-4 Clock Cycle and High/Low Timing Definition

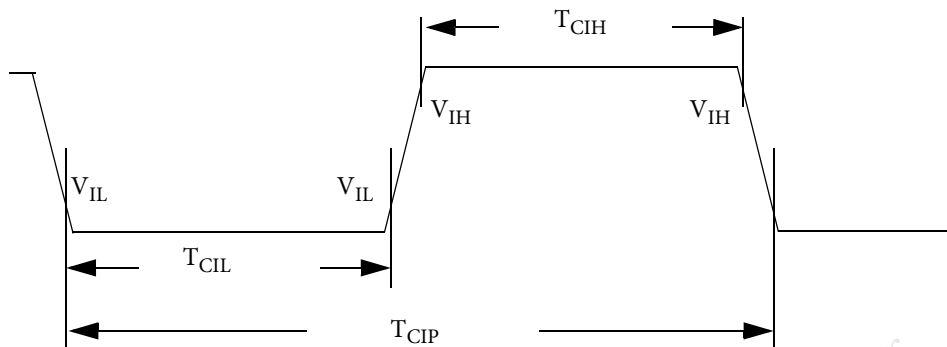


Figure 2-5 Single-Edge Clock to Data Setup/Hold Timing Definition

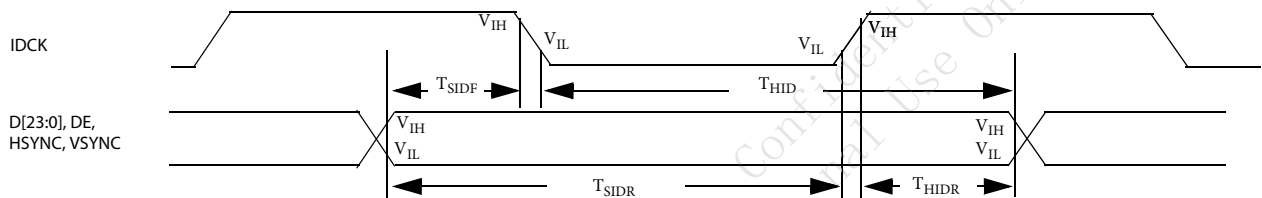


Figure 2-6 Dual-Edge Clock to Data Setup/Hold Timing Definition

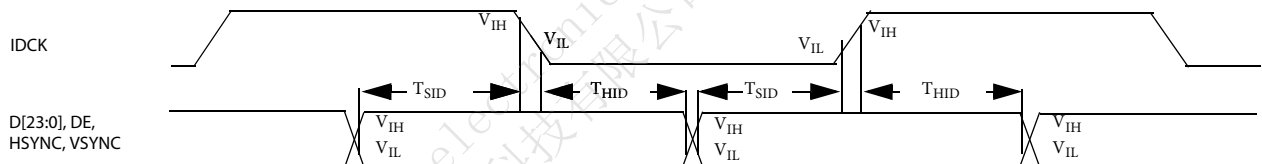


Figure 2-7 DE to HSYNC/VSYNC Delay Timing Definition

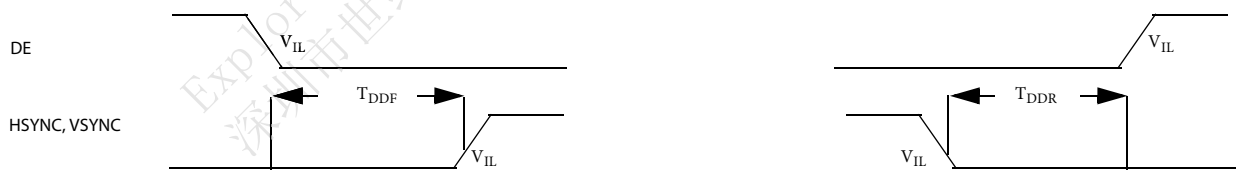


Figure 2-8 DE High/Low Timing Definition

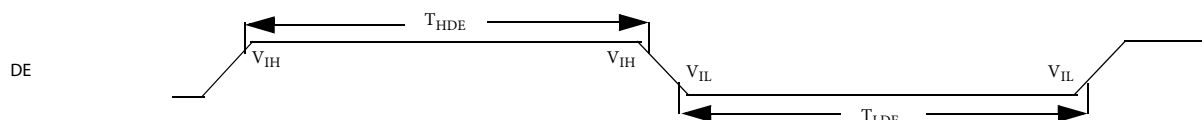
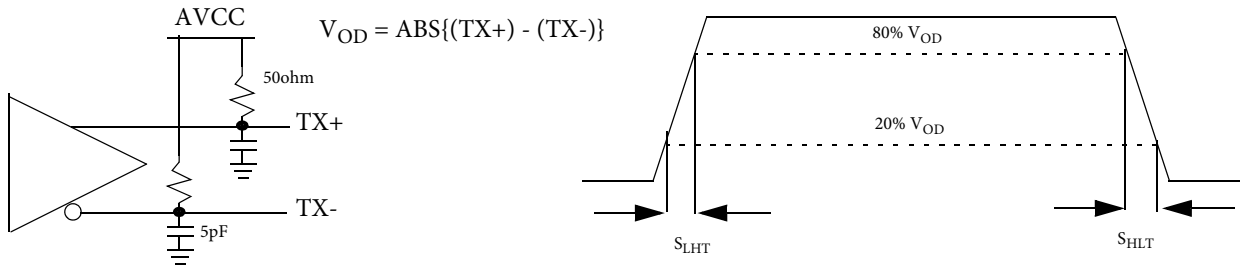


Figure 2-9 Differential Output Timing Definition



2.5 Data De-skew

Input clock to data setup/hold time can be adjusted through the use of the de-skew feature. It should be noted that it is the clock that is being adjusted. When DKEN=1, DK[3:1] can be used to vary the input setup/hold time by an amount T_{CD} given by the formula

$$T_{CD} = (DK[3:1] - 4) \times 200 \text{ ps.}$$

Where

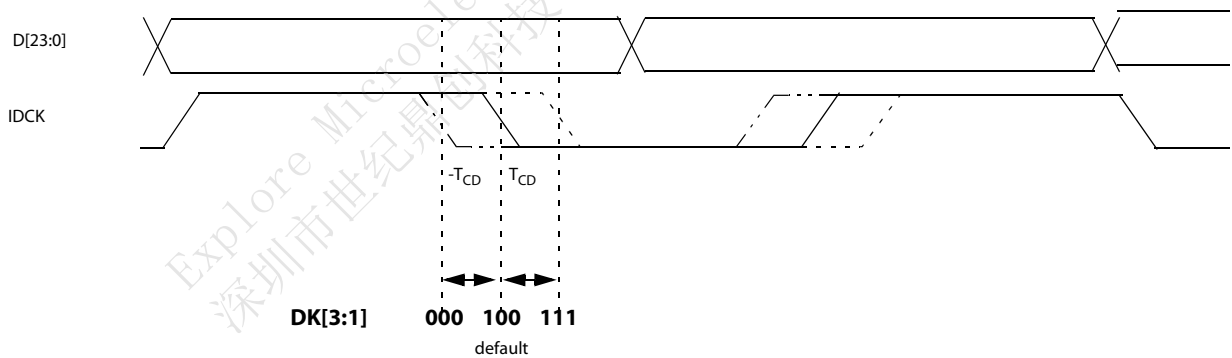
T_{CD} is the amount of setup/hold variation

DK[3:1] is the setting of the de-skew configuration pins or IIC registers

This feature can be used in both 12-bit and 24-bit mode.

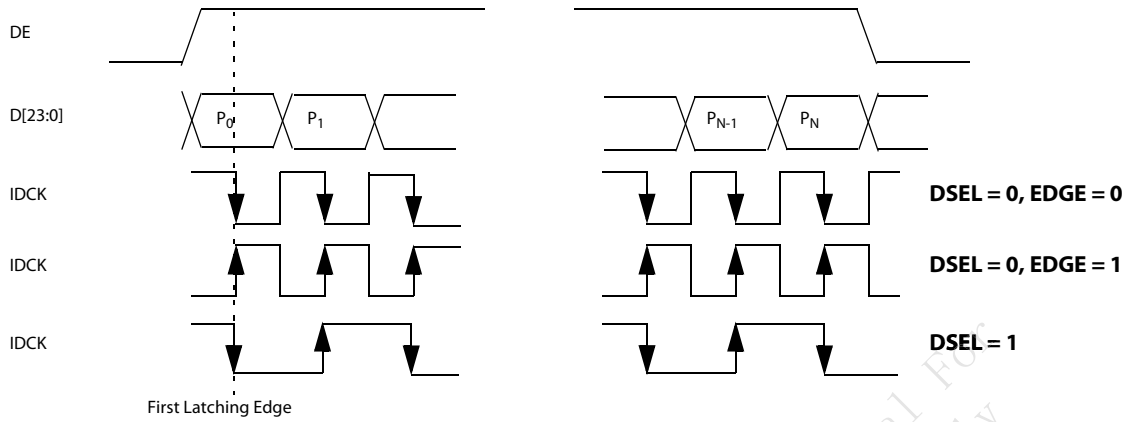
If Data De-skew is disabled, the default setting of $T_{CD}=0$ is used.

Figure 2-10 Single-Edge Clock to Data Setup/Hold Timing Definition



2.6 24-bit Data Mapping

Figure 2-11 24-bit Single/Dual Clock Edge Setting



Note: In Dual Clock Edge Mode, the transmitter will look at the first clock edge (either falling or rising) after DE goes HIGH to determine the first pixel data. In Embedded Sync mode, DE is extracted from EAV/SAV code according for CCIR-656 standard. EDGE pin has no affect in Dual Clock Edge Mode.

Table 2-7 24-bit Mode Data Mapping (BSEL = 1)^{1,2,3}

Pin Name	RGB	YCbCr444	YCbCr422
D23	R[7]	Cr[7]	Cb/Cr[11]
D22	R[6]	Cr[6]	Cb/Cr[10]
D21	R[5]	Cr[5]	Cb/Cr[9]
D20	R[4]	Cr[4]	Cb/Cr[8]
D19	R[3]	Cr[3]	Cb/Cr[7]
D18	R[2]	Cr[2]	Cb/Cr[6]
D17	R[1]	Cr[1]	Cb/Cr[5]
D16	R[0]	Cr[0]	Cb/Cr[4]
D15	G[7]	Cr[7]	Y[11]/EAV[7]/SAV[7]
D14	G[6]	Y[6]	Y[10]/EAV[6]/SAV[6]
D13	G[5]	Y[5]	Y[9]/EAV[5]/SAV[5]
D12	G[4]	Y[4]	Y[8]/EAV[4]/SAV[4]
D11	G[3]	Y[3]	Y[7]/EAV[3]/SAV[3]
D10	G[2]	Y[2]	Y[6]/EAV[2]/SAV[2]
D9	G[1]	Y[1]	Y[5]/EAV[1]/SAV[1]
D8	G[0]	Y[0]	Y[4]/EAV[0]/SAV[0]
D7	B[7]	Cb[7]	Cb/Cr[3]
D6	B[6]	Cb[6]	Cb/Cr[2]
D5	B[5]	Cb[5]	Cb/Cr[1]
D4	B[4]	Cb[4]	Cb/Cr[0]
D3	B[3]	Cb[3]	Y[3]
D2	B[2]	Cb[2]	Y[2]

Table 2-7 24-bit Mode Data Mapping (BSEL = 1)^{1,2,3}

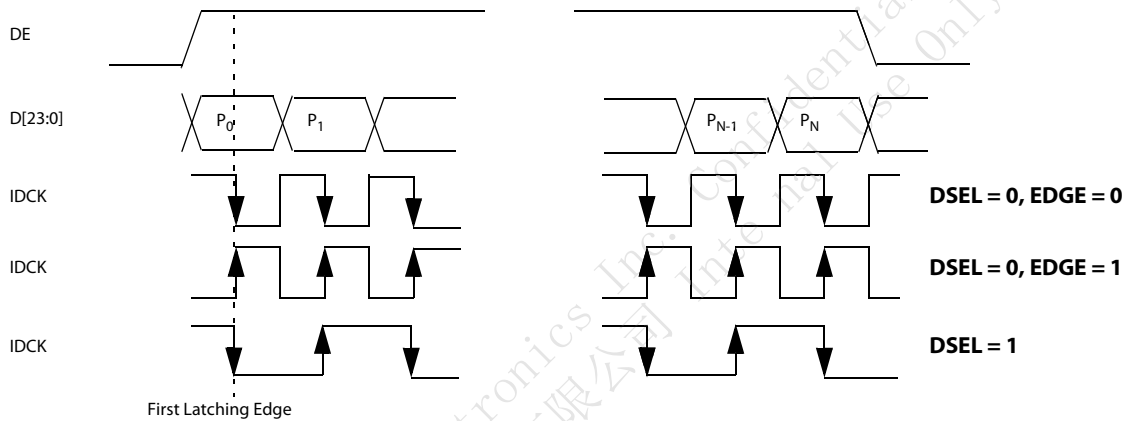
Pin Name	RGB	YCbCr444	YCbCr422
D1	B[1]	Cb[1]	Y[1]
D0	B[0]	Cb[0]	Y[0]

NOTES:

1. In this figure, clock edges represents by arrows signify the latching edge
2. In 24-bit YCbCr422 input, Cb data comes in first clock edge and Cr data comes in next clock edge
3. For less than 12-bit YCbCr422 input, the MSB data should be connected to input bit [11] and unused low input bits should be connected to logic 0
4. Bit significance with in a pixel component : [7:0] = [MSB:LSB]
5. In embedded sync mode, Hsync, Vsync and DE signals are extracted from EAV/SAV codes according to CCIR 656 standard.

2.7 12-bit Data Mapping

Figure 2-12 12-bit Single/Dual Clock Edge Setting



Note: The clock timing is the same as that in 24-bit mode except that the frequency of latching edge is 2 times of pixel frequency.

Table 2-8 12-bit Mode Data Mapping (BSEL = 0)^{1,2,3}

Pin Name	RGB444(FMT12 = 0)		YCbCr444(FMT12 = 0)		YCbCr422(FMT12 = 1)	
	1st clock	2nd clock	1st clock	2nd clock	1st clock	2nd clock
D15	-	-	-	-	Cb/Cr[11]/EAV[7]/SAV[7]	Y[11]/EAV[7]/SAV[7]
D14	-	-	-	-	Cb/Cr[10]/EAV[6]/SAV[6]	Y[10]/EAV[6]/SAV[6]
D13	-	-	-	-	Cb/Cr[9]/EAV[5]/SAV[5]	Y[9]/EAV[5]/SAV[5]
D12	-	-	-	-	Cb/Cr[8]/EAV[4]/SAV[4]	Y[8]/EAV[4]/SAV[4]
D11	G[3]	R[7]	Y[3]	Cr[7]	Cb/Cr[7]/EAV[3]/SAV[3]	Y[7]/EAV[3]/SAV[3]
D10	G[2]	R[6]	Y[2]	Cr[6]	Cb/Cr[6]/EAV[2]/SAV[2]	Y[6]/EAV[2]/SAV[2]
D9	G[1]	R[5]	Y[1]	Cr[5]	Cb/Cr[5]/EAV[1]/SAV[1]	Y[5]/EAV[1]/SAV[1]
D8	G[0]	R[4]	Y[0]	Cr[4]	Cb/Cr[4]/EAV[0]/SAV[0]	Y[4]/EAV[0]/SAV[0]
D7	B[7]	R[3]	Cb[7]	Cr[3]	-	-
D6	B[6]	R[2]	Cb[6]	Cr[2]	-	-

Table 2-8 12-bit Mode Data Mapping (BSEL = 0)^{1,2,3}

Pin Name	RGB444(FMT12 = 0)		YCbCr444(FMT12 = 0)		YCbCr422(FMT12 = 1)	
	1st clock	2nd clock	1st clock	2nd clock	1st clock	2nd clock
D5	B[5]	R[1]	Cb[5]	Cr[1]	-	-
D4	B[4]	R[0]	Cb[4]	Cr[0]	-	-
D3	B[3]	G[7]	Cb[3]	Y[7]	Cb/Cr[3]	Y[3]
D2	B[2]	G[6]	Cb[2]	Y[6]	Cb/Cr[2]	Y[2]
D1	B[1]	G[5]	Cb[1]	Y[5]	Cb/Cr[1]	Y[1]
D0	B[0]	G[4]	Cb[0]	Y[4]	Cb/Cr[0]	Y[0]

NOTES:

1. In this figure, clock edges represents by arrows signify the latching edge. The primary latch edge is indicated by the dark rows. The lower half of the pixel (L) is latched by the primary clock edge.
2. In 12-bit YCbCr422 input, Cb data comes in first clock edge, Y comes in 2nd and 4th clock edges and Cr data comes in 3rd clock edge
3. For less than 12-bit YCbCr422 input, the MSB data should be connected to input bit [11] and unused low input bits should be connected to logic 0
4. Bit significance with in a pixel component : [7:0] = [MSB:LSB]
5. In embedded sync mode, Hsync, Vsync and DE signals are extracted from EAV/SAV codes according to CCIR 656 standard.
6. Unused pins should not left floating.

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Appendix A Package

Figure A-1 LQFP-64 Footprint Diagram

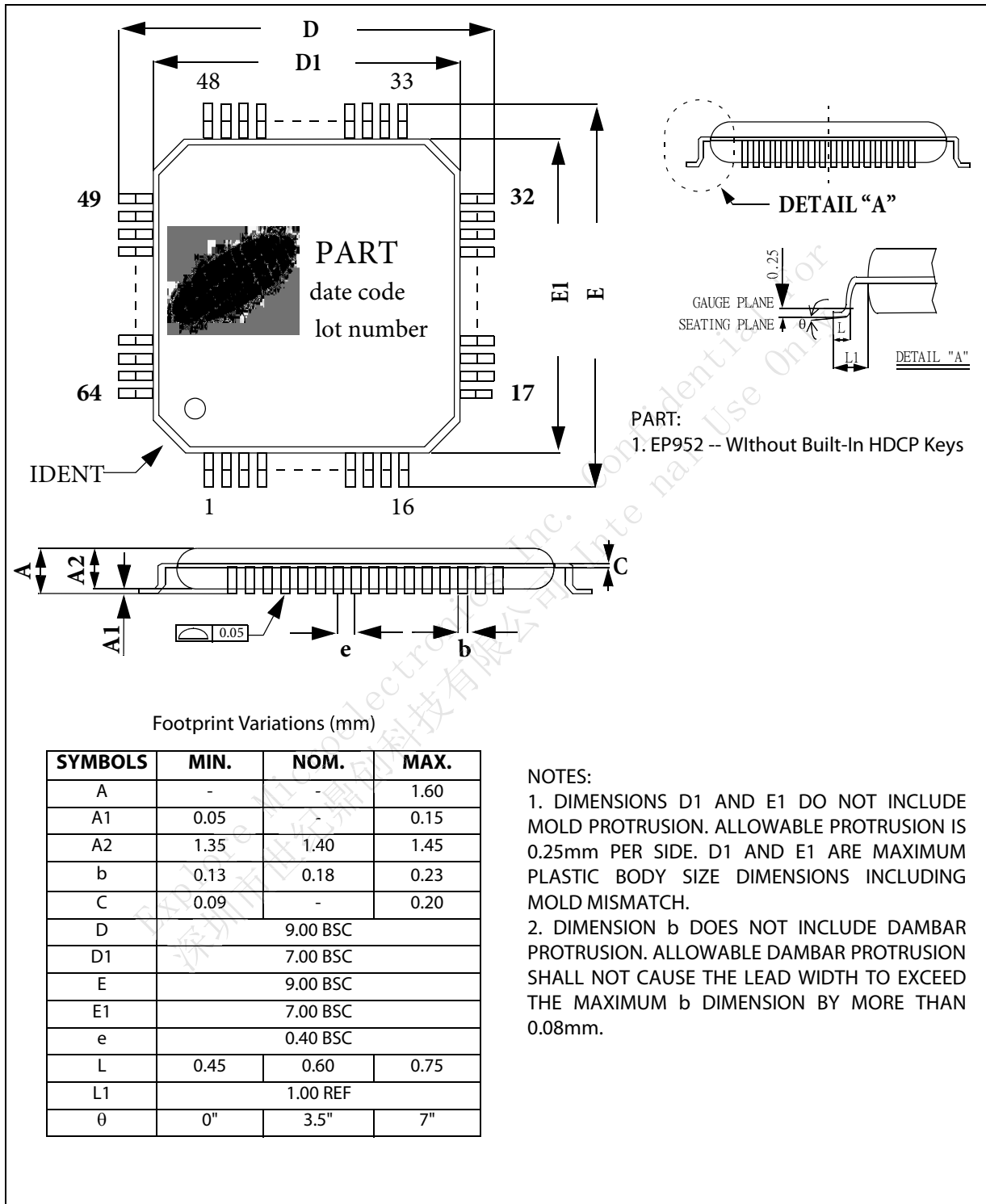


Figure A-2 BGA-64 Footprint Diagram

